



H61H2-LM5

Rev : 0.1

ECS
CONFIDENTIAL

TABLE OF CONTENTS


Page	Index
1	Cover Page
2	Block Diagram
3	GPIO Function Map
4	CPU - DMI/FDI/PEG
5	CPU - MISC
6	CPU - DDR3
7	CPU - PWR
8	CPU - GND, CPU_RST_L
9	DDR3 - CHA DIMM
10	DDR3 - CHB DIMM
11	DDR3 - VREF
12	PCH - DMI/PCH-PE/USB
13	PCH - SATA, SATA CONN
14	PCH - MISC, Strap Function
15	PCH - CLK IO
16	PCH - FDI,CLR_CMOS,ROM,SMbus
17	PCH - DVI/VGA
18	PCH - PWR
19	PCH - GND,VGA CONN
20	PCIE*16,PCIE*1 Slot
21	P21 PCI Bridge (IT8893E-FX)
22	P22 PCI Slot
23	LAN(RTL8111F-VB/8111E-VB)
24	USBLAN Connector
25	Audio (ALC662-VD)

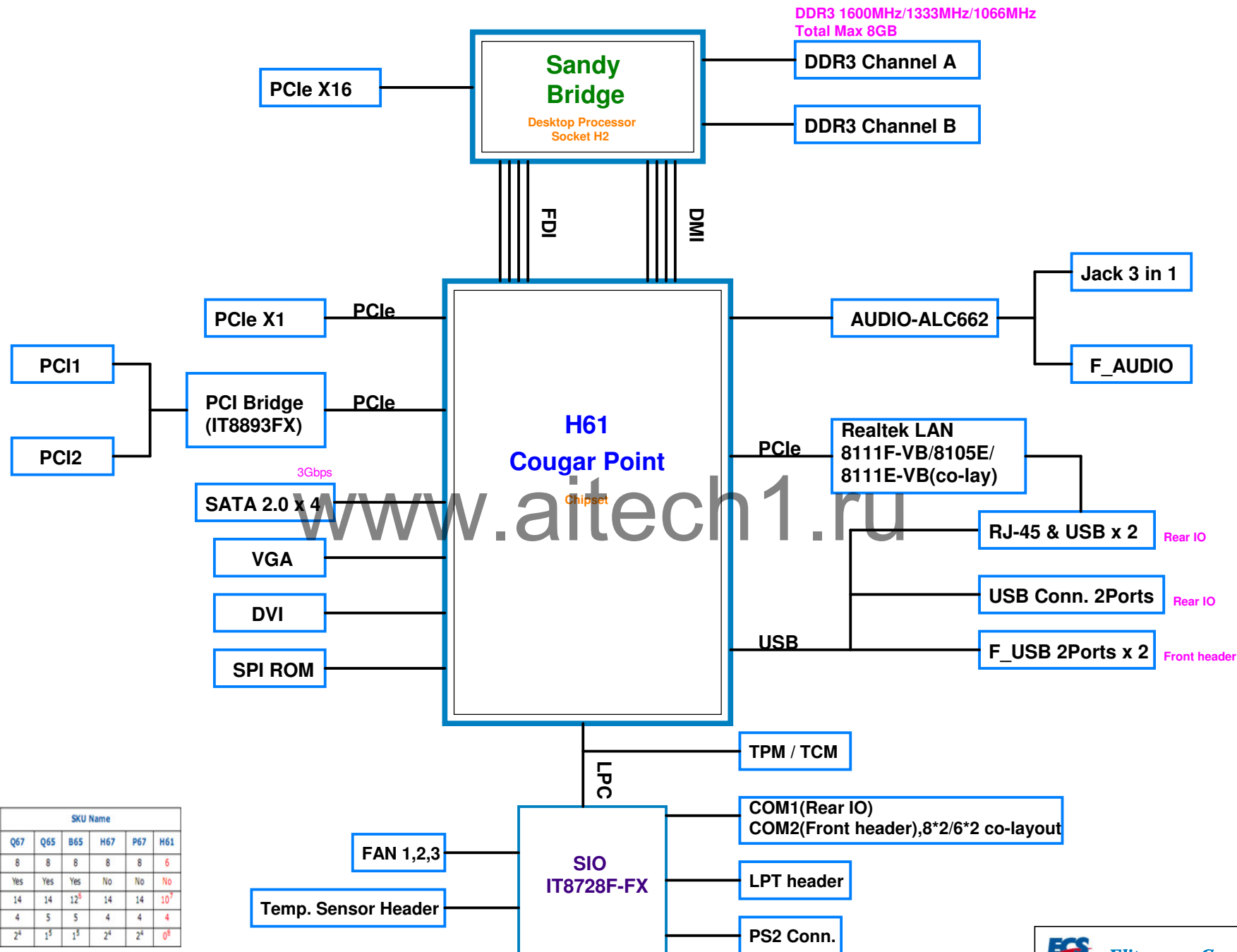
REVISION HISTORY:

Rev	Date	Notes
26		Audio - CONN&HDR
27		USB - PWR&CONN&HDR
28		LPC Device
29		SIO (IT8728F-FX)
30		FAN,COM,CASE_OPEN,THERMAL
31		F_PANEL,BUZ,PS2,LPT
32		DC/DC 3VDUAL
33		DC/DC V1P05_PCH,ME/V1P8_SFR
34		DC/DC VDIMM/DDR_VTT/5VDUAL
35		DC/DC VCCSA, ATXPWR
36		DC/DC V_CPUVTT
37		DC/DC V_CORE/VAXG1
38		DC/DC V_CORE/VAXG2
39		XDP
40		Deep Sleep Well
41		104 & STRAPPING
42		Power Delivery
43		Power Sequence, Reset Diagram
44		Clock Distribution

Note:

design by
428971_428971_Sugar Bay and Bromolow-WS_PDQ_Rev2_0_December 2010
443554_443554_Intel 6 Series Chipset and Intel C200 Series Chipset_EDS_Rev1_5_January 2011

 Elitegroup Computer Systems		
Title Cover Page		
Size Custom	Document Number H61H2-LM5	Rev V0.1
Date: Friday, March 02, 2012	Sheet 1	of 44



Feature Set	SKU Name					
	Q67	Q65	B65	H67	P67	H61
PCI Express* 2.0 Ports	8	8	8	8	8	6
PCI Interface	Yes	Yes	Yes	No	No	No
USB 2.0 Ports	14	14	12 ⁵	14	14	10 ⁷
SATA Ports (3.0 Gb/s & 1.5 Gb/s only)	4	5	5	4	4	4
SATA Ports (6.0 Gb/s & 3.0 Gb/s & 1.5 Gb/s)	2 ⁴	1 ⁵	1 ⁵	2 ⁴	2 ⁴	0 ⁸

4. SATA 6 Gb/s support on Port 0 and Port 1. SATA Ports also Support 1.5 Gb/s and 3.0 Gb/s.
5. SATA 6 Gb/s support on Port 0 only. SATA Port also Support 1.5 Gb/s and 3.0 Gb/s.
6. USB ports 6 and 7 are disable.
7. USB ports 6, 7, 12 and 13 are disabled
8. SATA Ports 2 and Ports 3 are disabled

PCH-GPIO function

Data: 2012 / 01 / 30

Pin Name	Power Well	Usage	Default Status
GPIO51	VCC3	GPIO	GPI
GPIO53	VCC3	GPIO	GPI
GPIO55	VCC3	GPIO	GPI
GPIO50	VCC3	GPIO	GPI
GPIO52	VCC3	GPIO	GPI
GPIO54	VCC3	GPIO	GPI
GPIO59	3VSB	USB_OC_L0	Native
GPIO40	3VSB	USB_OC_L1	Native
GPIO41	3VSB	USB_OC_L2	Native
GPIO42	3VSB	USB_OC_L3	Native
GPIO43	3VSB	USB_OC_L4	Native
GPIO9	3VSB	USB_OC_L5	Native
GPIO10	3VSB	USB_OC_L6	Native
GPIO14	3VSB	USB_OC_L7	Native
GPIO17	VCC3	GP17_BOMDET1	GPI
GPIO1	VCC3	GP1_BOMDET2	GPI
GPIO6	VCC3	GPIO6_KMDET	GPI
GPIO7	VCC3	GPIO	GPI
GPIO68	VCC3	GPIO68_USBDET1	GPI
GPIO69	VCC3	GPIO69_USBDET2	GPI
GPIO70	VCC3	GPIO70_LPTDET3	GPI
GPIO71	VCC3	GP71_BOMDET3	GPI
GPIO22	VCC3	CLR_CMOS_GP22	GPI
GPIO38	VCC3	GPIO38_TCM	GPI
GPIO39	VCC3	GPIO39_CASE0	GPI
GPIO48	VCC3	GPIO48_CASE1	GPI
GPIO21	VCC3	GPIO21_COM2_DET	GPI
GPIO32	VCC3	TCM_DIS_L	GPO
GPIO34	VCC3	GPIO34_TCM_PST_L	GPI
GPIO35	VCC3	TP_VGA	GPO
GPIO12	+DIMM_5VDUAL	POWER LED	Native
GPIO13	3VSB	LPC_PME_L	GPI
GPIO45	3VSB	GP45_BOMDET4	GPI
GPIO72	3VSB	GP72_BOMDET5	GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO24	3VSB	PCH_SKTOCC_L	GPO
GPIO61	VCC3	LPCPD_L	Native
GPIO60	3VSB	LAN_OE	Native
GPIO74	3VSB	LAN_SEL	Native
GPIO57	3VSB	LAN_SEL	Native

NOTE: GPIO60,74,57 Reserve for Dual LAN solution

SIO-GPIO function

Data: 2012 / 01 / 30

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	SIO_BEEP	
GP22	3VSB	Power LED	
GP40	3VSB	5VDUAL control	

Chipset PCIE INT Fuction

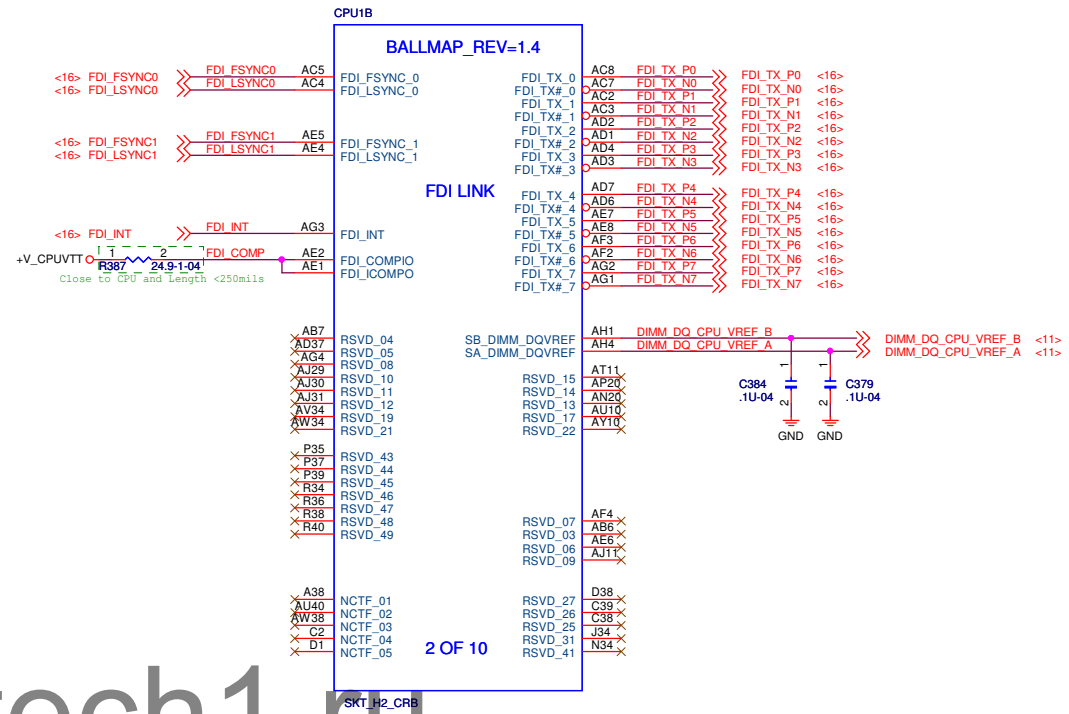
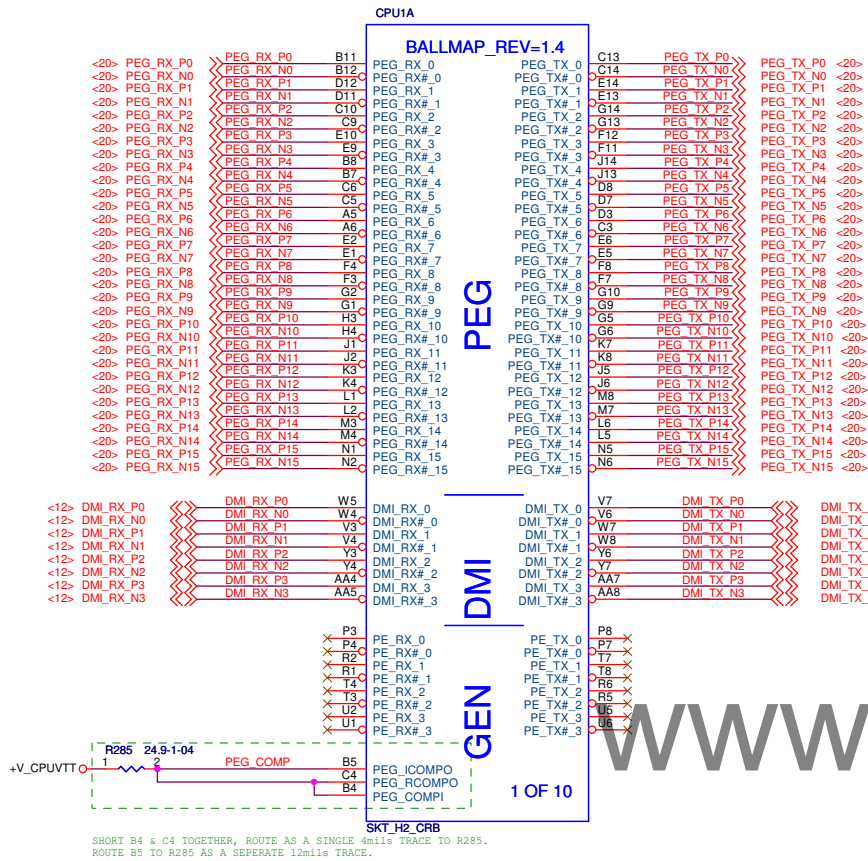
Data: 2012 / 01 / 30

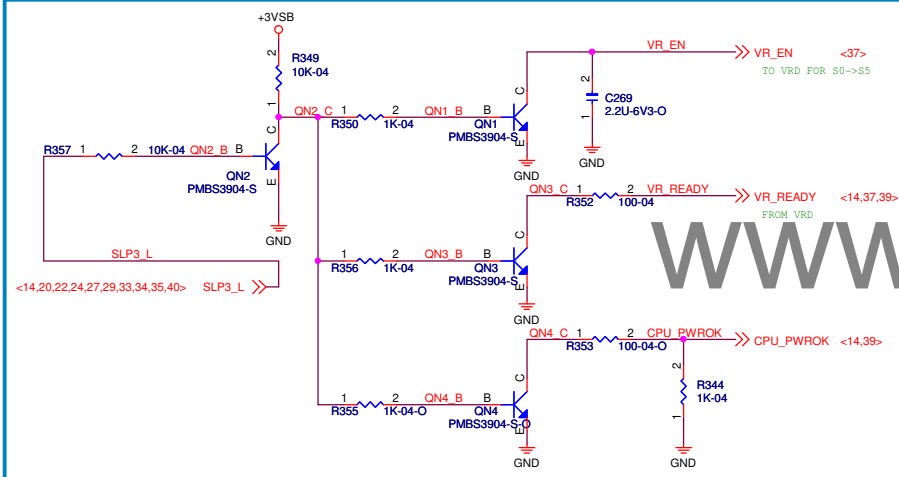
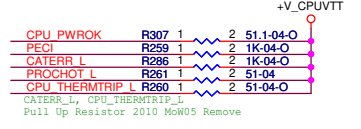
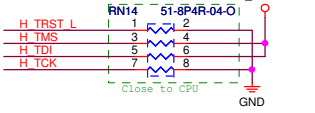
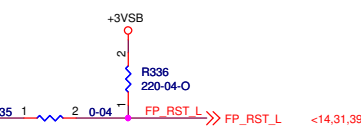
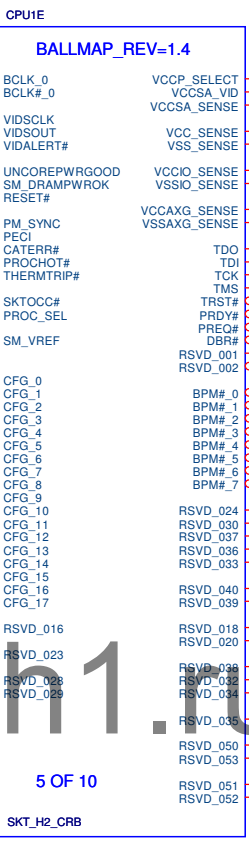
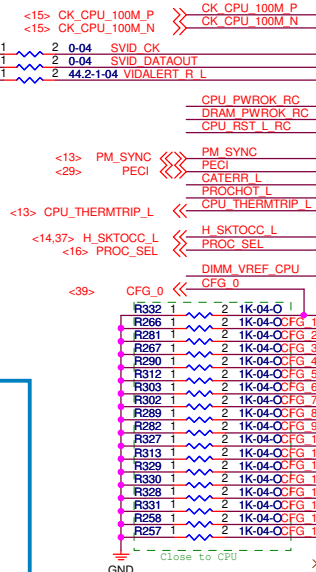
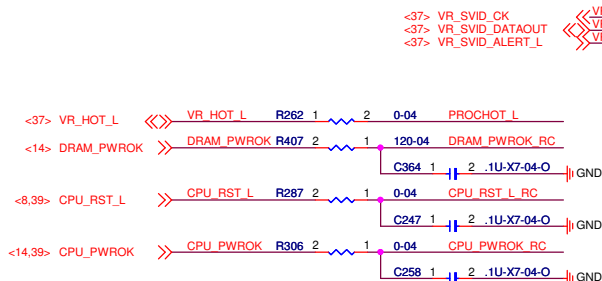
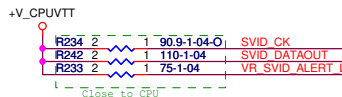
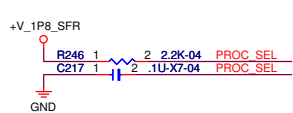
Fucntion	INT Port	PCIEX1 port	Chipset
PCIE to PCI	INTC#	PCI Express #3 Pin	IT8893FX
PCI-E Slot	INTD#	PCI Express #4 Pin	PCI-E Slot
LAN	INTA#	PCI Express #5 Pin	Realtek LAN
Sata Controller	INTB#	N/A	H61 intergrated

Chipset PCI Fuction

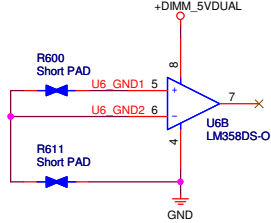
Data: 2012 / 01 / 30

Fucntion	INT Port	IDSEL	Chipset
PCI1	A/B/C/D	AD16	N/A
PCI2	B/C/D/A	AD17	N/A

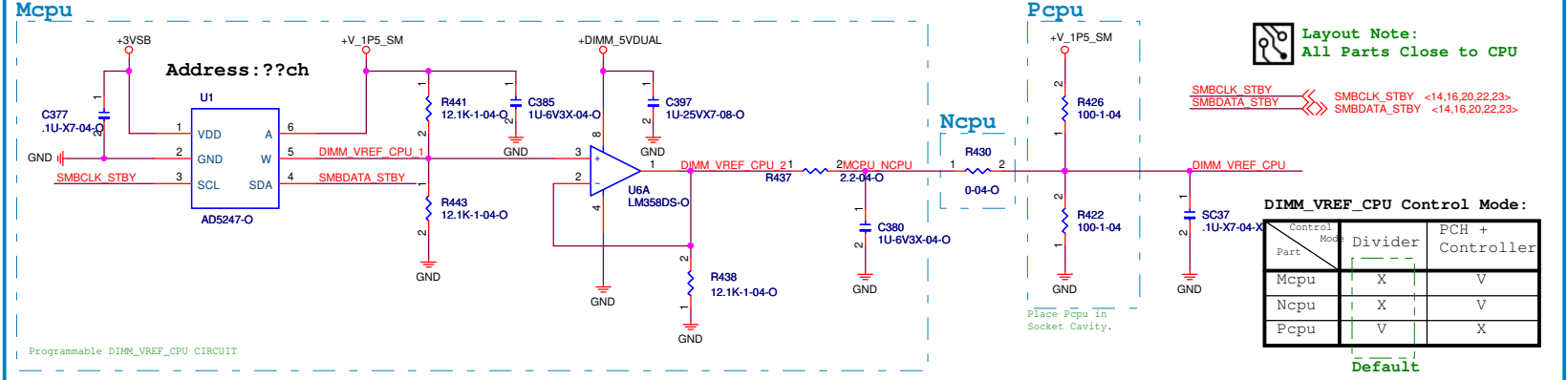




Power Down Sequencing Circuit



5 OF 10



DIMM_VREF_CPU Control Circuit

Layout Note:
All Parts Close to CPU

SMBCLK_STBY <<> SMBCLK_STBY <14,16,20,22,23>
SMBDATA_STBY <<> SMBDATA_STBY <14,16,20,22,23>

DIMM_VREF_CPU Control Mode:

Control Mode	Divider	PCH + Controller
Mcpu	X	V
Ncpu	X	V
Pcpu	V	X

Default

CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG_[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8,X4,X4



<9> M_DATA_A[0..63]	← M_DATA A[0..63]
<9> M_DQS_A_P[0..7]	← M DQS A P[0..7]
<9> M_DQS_A_N[0..7]	← M DQS A N[0..7]
<9> M_MA_A[0..15]	← M MA A[0..15]
<9> M_BS_A[0..2]	← M BS A[0..2]
<9> M_CS_A_L[0..1]	← M CS A L[0..1]
<9> M_CKE_A[0..1]	← M CKE A[0..1]
<9> M_ODT_A[0..1]	← M ODT A[0..1]
<9> M_CLK_A_P[0..1]	← M CLK A P[0..1]
<9> M_CLK_A_N[0..1]	← M CLK A N[0..1]
<9> M_WE_A_L	← M WE A L
<9> M_CAS_A_L	← M CAS A L
<9> M_RAS_A_L	← M RAS A L

DDR3 CH.A

<9,10> DDR3_DRAMRST_L ← DDR3_DRAMRST_L

<10> M_DATA_B[0..63]	← M_DATA B[0..63]
<10> M_DQS_B_P[0..7]	← M DQS B P[0..7]
<10> M_DQS_B_N[0..7]	← M DQS B N[0..7]
<10> M_MA_B[0..15]	← M MA B[0..15]
<10> M_BS_B[0..2]	← M BS B[0..2]
<10> M_CS_B_L[0..1]	← M CS B L[0..1]
<10> M_CKE_B[0..1]	← M CKE B[0..1]
<10> M_ODT_B[0..1]	← M ODT B[0..1]
<10> M_CLK_B_P[0..1]	← M CLK B P[0..1]
<10> M_CLK_B_N[0..1]	← M CLK B N[0..1]
<10> M_WE_B_L	← M WE B L
<10> M_CAS_B_L	← M CAS B L
<10> M_RAS_B_L	← M RAS B L

DDR3 CH.B

M_DATA A0	AJ3	SA_DQ_0
M_DATA A1	AJ4	SA_DQ_1
M_DATA A2	AL3	SA_DQ_2
M_DATA A3	AL4	SA_DQ_3
M_DATA A4	AJ2	SA_DQ_4
M_DATA A5	AJ1	SA_DQ_5
M_DATA A6	AL1	SA_DQ_6
M_DATA A7	AL1	SA_DQ_7
M_DATA A8	AN1	SA_DQ_8
M_DATA A9	AN4	SA_DQ_9
M_DATA A10	AR3	SA_DQ_10
M_DATA A11	AR4	SA_DQ_11
M_DATA A12	AN2	SA_DQ_12
M_DATA A13	AN3	SA_DQ_13
M_DATA A14	AR2	SA_DQ_14
M_DATA A15	AR1	SA_DQ_15
M_DATA A16	AV2	SA_DQ_16
M_DATA A17	AV3	SA_DQ_17
M_DATA A18	AV5	SA_DQ_18
M_DATA A19	AW5	SA_DQ_19
M_DATA A20	AU2	SA_DQ_20
M_DATA A21	AU3	SA_DQ_21
M_DATA A22	AU5	SA_DQ_22
M_DATA A23	AV6	SA_DQ_23
M_DATA A24	AY7	SA_DQ_24
M_DATA A25	AU7	SA_DQ_25
M_DATA A26	AV9	SA_DQ_26
M_DATA A27	AU9	SA_DQ_27
M_DATA A28	AV7	SA_DQ_28
M_DATA A29	AW7	SA_DQ_29
M_DATA A30	AW9	SA_DQ_30
M_DATA A31	AY9	SA_DQ_31
M_DATA A32	AU35	SA_DQ_32
M_DATA A33	AW37	SA_DQ_33
M_DATA A34	AU39	SA_DQ_34
M_DATA A35	AU36	SA_DQ_35
M_DATA A36	AW35	SA_DQ_36
M_DATA A37	AY36	SA_DQ_37
M_DATA A38	AU38	SA_DQ_38
M_DATA A39	AU37	SA_DQ_39
M_DATA A40	AR40	SA_DQ_40
M_DATA A41	AR37	SA_DQ_41
M_DATA A42	AN38	SA_DQ_42
M_DATA A43	AN37	SA_DQ_43
M_DATA A44	AR39	SA_DQ_44
M_DATA A45	AR38	SA_DQ_45
M_DATA A46	AN39	SA_DQ_46
M_DATA A47	AN40	SA_DQ_47
M_DATA A48	AL40	SA_DQ_48
M_DATA A49	AL37	SA_DQ_49
M_DATA A50	AJ38	SA_DQ_50
M_DATA A51	AJ37	SA_DQ_51
M_DATA A52	AL38	SA_DQ_52
M_DATA A53	AL38	SA_DQ_53
M_DATA A54	AJ40	SA_DQ_54
M_DATA A55	AG40	SA_DQ_55
M_DATA A56	AG37	SA_DQ_56
M_DATA A57	AG37	SA_DQ_57
M_DATA A58	AE38	SA_DQ_58
M_DATA A59	AE37	SA_DQ_59
M_DATA A60	AG39	SA_DQ_60
M_DATA A61	AG38	SA_DQ_61
M_DATA A62	AE39	SA_DQ_62
M_DATA A63	AE40	SA_DQ_63

M_DQS A P0	AK3	SA_DQS_0
M_DQS A P1	AP3	SA_DQS_1
M_DQS A P2	AW4	SA_DQS_2
M_DQS A P3	AV8	SA_DQS_3
M_DQS A P4	AV37	SA_DQS_4
M_DQS A P5	AP38	SA_DQS_5
M_DQS A P6	AK38	SA_DQS_6
M_DQS A P7	AF38	SA_DQS_7

M_DQS A N0	AK2	SA_DQS#_0
M_DQS A N1	AP2	SA_DQS#_1
M_DQS A N2	AV4	SA_DQS#_2
M_DQS A N3	AW8	SA_DQS#_3
M_DQS A N4	AV36	SA_DQS#_4
M_DQS A N5	AP39	SA_DQS#_5
M_DQS A N6	AK39	SA_DQS#_6
M_DQS A N7	AF39	SA_DQS#_7

BALLMAP_REV=1.4

SM_DRAMRST#

SA_DQS_8

SA_DQS#_8

SA_ECC_CB_0

SA_ECC_CB_1

SA_ECC_CB_2

SA_ECC_CB_3

SA_ECC_CB_4

SA_ECC_CB_5

SA_ECC_CB_6

SA_ECC_CB_7

SA_ECC_CB_8

SA_ECC_CB_9

SA_ECC_CB_10

SA_ECC_CB_11

SA_ECC_CB_12

SA_ECC_CB_13

SA_ECC_CB_14

SA_ECC_CB_15

SA_ECC_CB_16

SA_ECC_CB_17

SA_ECC_CB_18

SA_ECC_CB_19

SA_ECC_CB_20

SA_ECC_CB_21

SA_ECC_CB_22

SA_ECC_CB_23

SA_ECC_CB_24

SA_ECC_CB_25

SA_ECC_CB_26

SA_ECC_CB_27

SA_ECC_CB_28

SA_ECC_CB_29

SA_ECC_CB_30

SA_ECC_CB_31

SA_ECC_CB_32

SA_ECC_CB_33

SA_ECC_CB_34

SA_ECC_CB_35

SA_ECC_CB_36

SA_ECC_CB_37

SA_ECC_CB_38

SA_ECC_CB_39

SA_ECC_CB_40

SA_ECC_CB_41

SA_ECC_CB_42

SA_ECC_CB_43

SA_ECC_CB_44

SA_ECC_CB_45

SA_ECC_CB_46

SA_ECC_CB_47

SA_ECC_CB_48

SA_ECC_CB_49

SA_ECC_CB_50

SA_ECC_CB_51

SA_ECC_CB_52

SA_ECC_CB_53

SA_ECC_CB_54

SA_ECC_CB_55

SA_ECC_CB_56

SA_ECC_CB_57

SA_ECC_CB_58

SA_ECC_CB_59

SA_ECC_CB_60

SA_ECC_CB_61

SA_ECC_CB_62

SA_ECC_CB_63

SA_ECC_CB_64

SA_ECC_CB_65

SA_ECC_CB_66

SA_ECC_CB_67

SA_ECC_CB_68

SA_ECC_CB_69

SA_ECC_CB_70

SA_ECC_CB_71

SA_ECC_CB_72

SA_ECC_CB_73

SA_ECC_CB_74

SA_ECC_CB_75

SA_ECC_CB_76

SA_ECC_CB_77

SA_ECC_CB_78

SA_ECC_CB_79

SA_ECC_CB_80

SA_ECC_CB_81

SA_ECC_CB_82

SA_ECC_CB_83

SA_ECC_CB_84

SA_ECC_CB_85

SA_ECC_CB_86

SA_ECC_CB_87

SA_ECC_CB_88

SA_ECC_CB_89

SA_ECC_CB_90

SA_ECC_CB_91

SA_ECC_CB_92

SA_ECC_CB_93

SA_ECC_CB_94

SA_ECC_CB_95

SA_ECC_CB_96

SA_ECC_CB_97

SA_ECC_CB_98

SA_ECC_CB_99

SA_ECC_CB_100

SA_ECC_CB_101

SA_ECC_CB_102

SA_ECC_CB_103

SA_ECC_CB_104

SA_ECC_CB_105

SA_ECC_CB_106

SA_ECC_CB_107

SA_ECC_CB_108

SA_ECC_CB_109

SA_ECC_CB_110

SA_ECC_CB_111

SA_ECC_CB_112

SA_ECC_CB_113

SA_ECC_CB_114

SA_ECC_CB_115

SA_ECC_CB_116

SA_ECC_CB_117

SA_ECC_CB_118

SA_ECC_CB_119

SA_ECC_CB_120

SA_ECC_CB_121

SA_ECC_CB_122

SA_ECC_CB_123

SA_ECC_CB_124

SA_ECC_CB_125

SA_ECC_CB_126

SA_ECC_CB_127

SA_ECC_CB_128

SA_ECC_CB_129

SA_ECC_CB_130

SA_ECC_CB_131

SA_ECC_CB_132

SA_ECC_CB_133

SA_ECC_CB_134

SA_ECC_CB_135

SA_ECC_CB_136

SA_ECC_CB_137

SA_ECC_CB_138

SA_ECC_CB_139

SA_ECC_CB_140

SA_ECC_CB_141

SA_ECC_CB_142

SA_ECC_CB_143

SA_ECC_CB_144

SA_ECC_CB_145

SA_ECC_CB_146

SA_ECC_CB_147

SA_ECC_CB_148

SA_ECC_CB_149

SA_ECC_CB_150

SA_ECC_CB_151

SA_ECC_CB_152

SA_ECC_CB_153

SA_ECC_CB_154

SA_ECC_CB_155

SA_ECC_CB_156

SA_ECC_CB_157

SA_ECC_CB_158

SA_ECC_CB_159

SA_ECC_CB_160

SA_ECC_CB_161

SA_ECC_CB_162

SA_ECC_CB_163

SA_ECC_CB_164

SA_ECC_CB_165

SA_ECC_CB_166

SA_ECC_CB_167

SA_ECC_CB_168

SA_ECC_CB_169

SA_ECC_CB_170

SA_ECC_CB_171

SA_ECC_CB_172

SA_ECC_CB_173

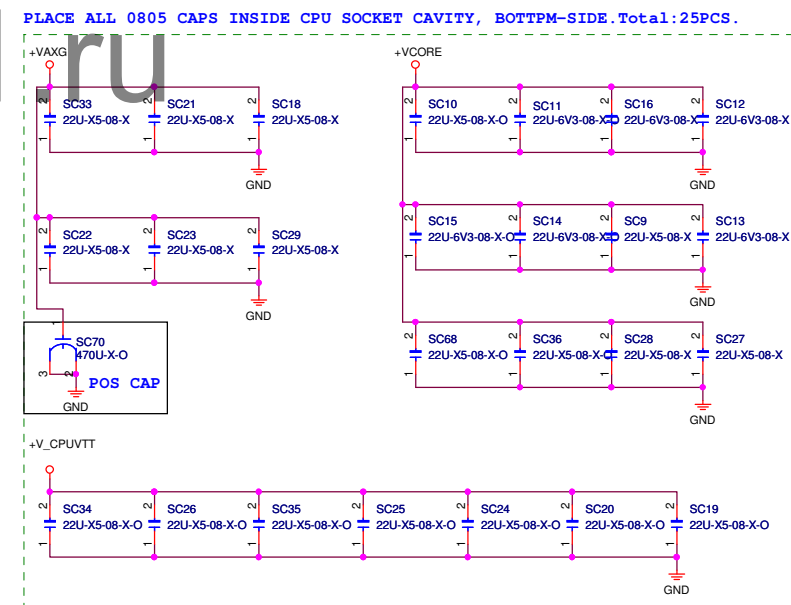
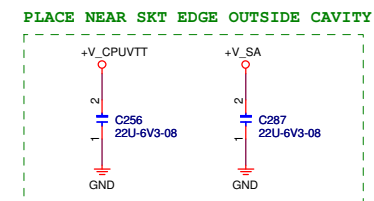
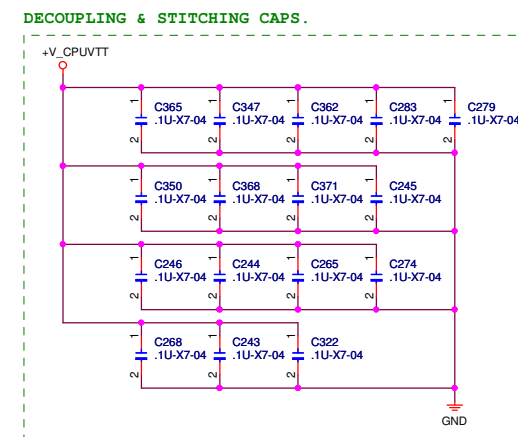
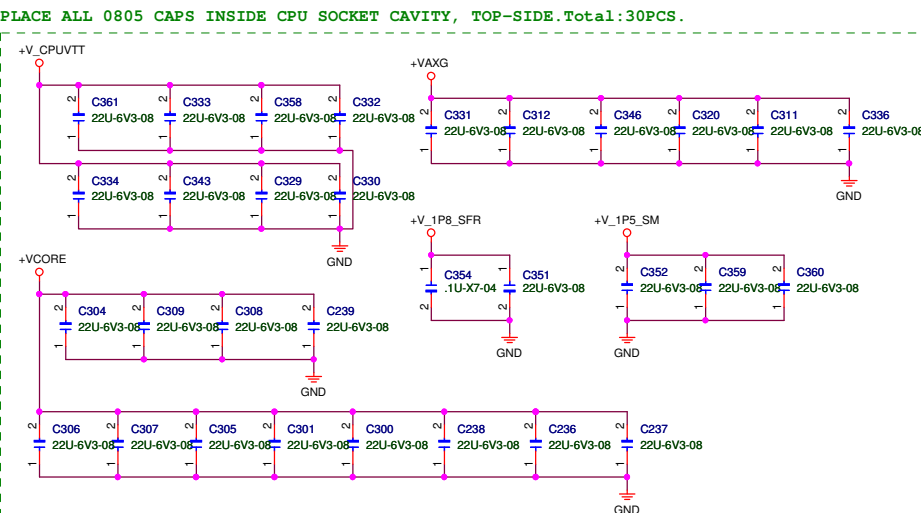
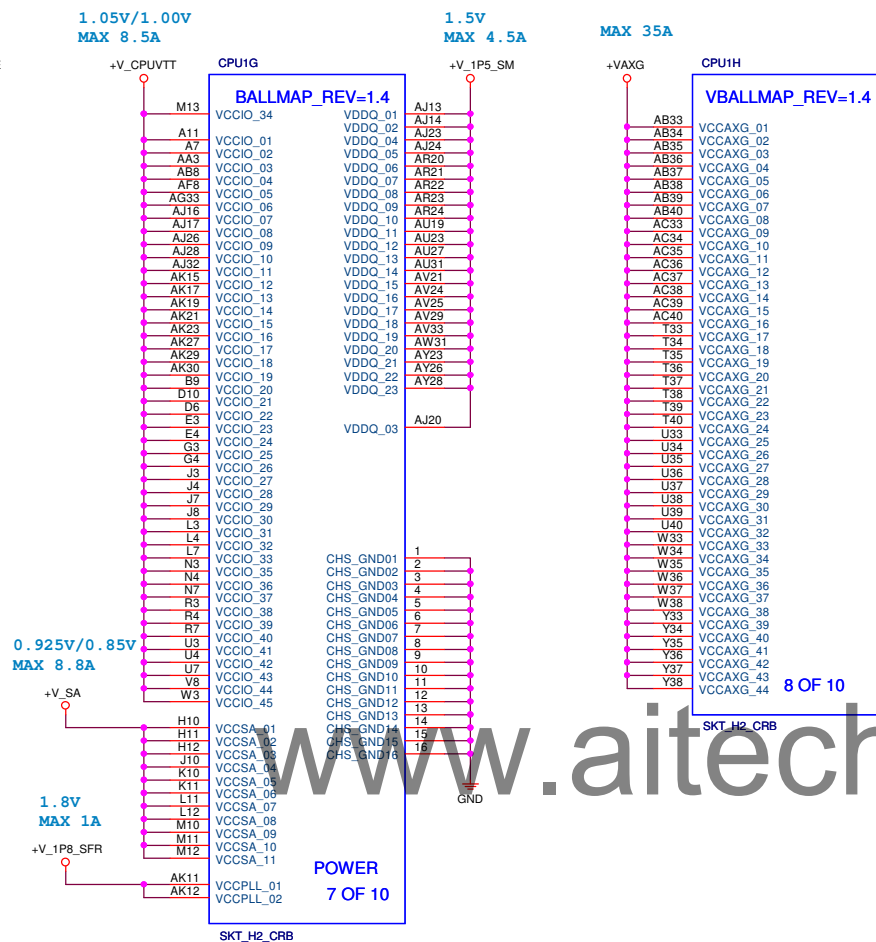
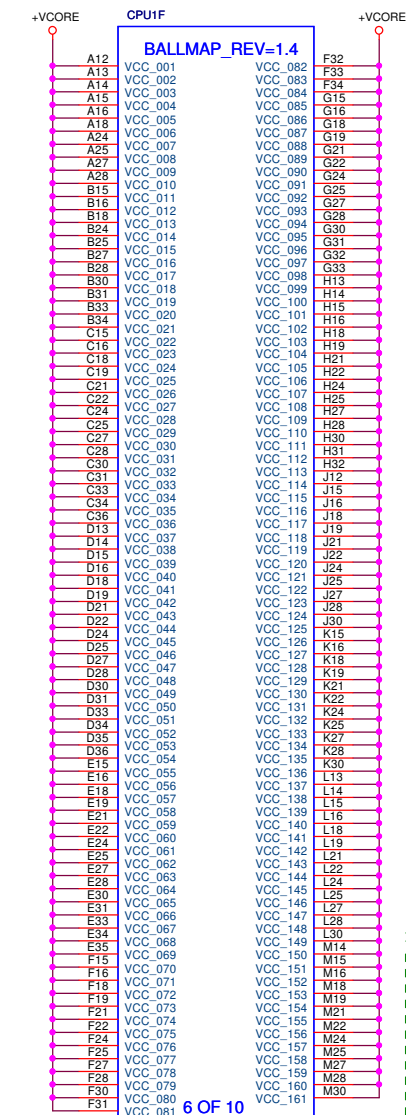
SA_ECC_CB_174

SA_ECC_CB_175

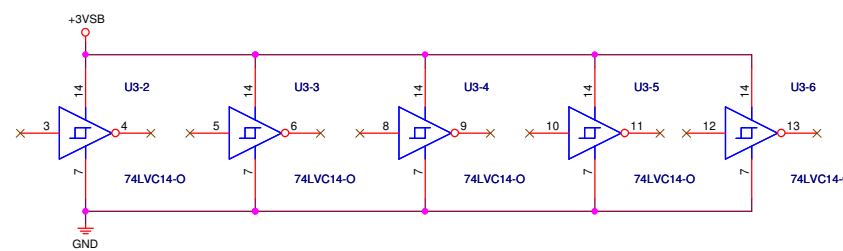
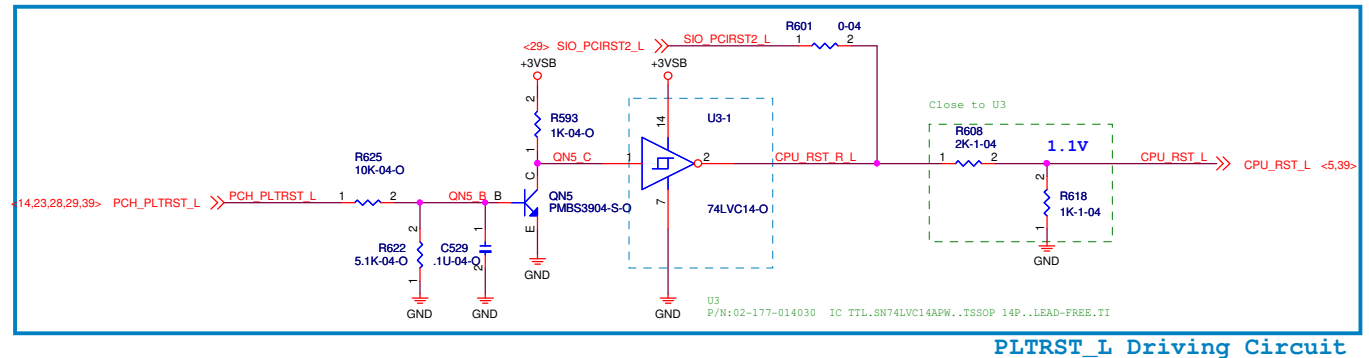
SA_ECC_CB_176

SA_ECC_CB_177

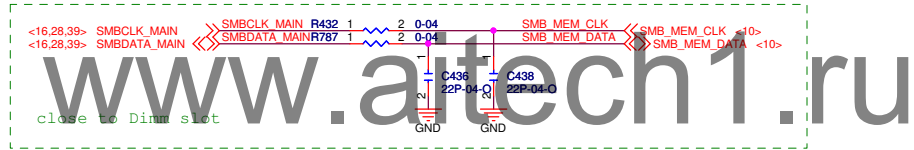
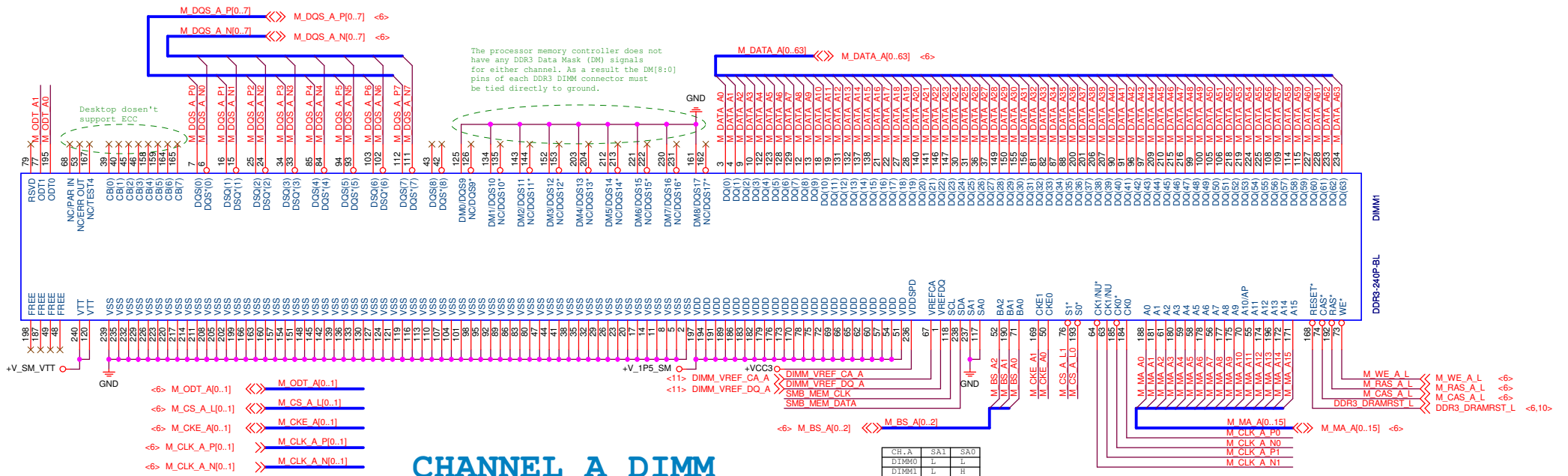
SA_ECC_CB_1



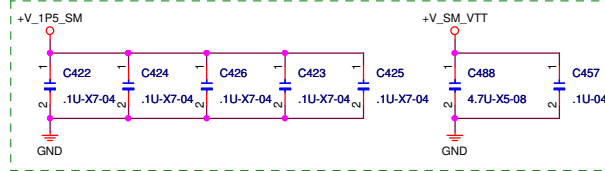
CPU1I			CPU1J		
BALLMAP_REV=1.4			BALLMAP_REV=1.4		
A17	VSS_001	AM27	AV11	VSS_181	G8
A23	VSS_002	AM3	AV14	VSS_182	H1
A26	VSS_003	AM30	AV17	VSS_183	H17
A29	VSS_004	AM36	AV3	VSS_184	H2
AA35	VSS_005	AM37	AV35	VSS_185	H20
AA33	VSS_006	AM38	AV38	VSS_186	H23
AA34	VSS_007	AM39	AV6	VSS_187	H26
AA35	VSS_008	AM4	AW10	VSS_188	H29
AA36	VSS_009	AM40	AW11	VSS_189	H33
AA37	VSS_010	AM5	AW14	VSS_190	H35
AA38	VSS_011	AN10	AW16	VSS_191	H37
AA6	VSS_012	AN11	AW36	VSS_192	H39
AB5	VSS_013	AN14	AW6	VSS_193	H5
AC1	VSS_014	AN17	AY11	VSS_194	H6
AC6	VSS_015	AN19	AY14	VSS_195	H9
AD33	VSS_016	AN22	AY18	VSS_196	J11
AD36	VSS_017	AN24	AY35	VSS_197	J17
AD38	VSS_018	AN30	AY6	VSS_198	J23
AD39	VSS_019	AN31	AY8	VSS_199	J26
AD40	VSS_020	AN32	B10	VSS_200	J29
AD5	VSS_021	AN33	B13	VSS_201	J32
AD8	VSS_022	AN34	B14	VSS_202	K1
AE3	VSS_023	AN35	B17	VSS_203	K12
AE33	VSS_024	AN36	B23	VSS_204	K13
AE36	VSS_025	AN5	B26	VSS_205	K14
AF1	VSS_026	AN6	B29	VSS_206	K17
AF34	VSS_027	AN7	B35	VSS_207	K2
AF36	VSS_028	AN8	B38	VSS_208	K20
AF37	VSS_029	AN9	B6	VSS_209	K23
AF40	VSS_030	AP1	B6	VSS_210	K26
AF5	VSS_031	AP11	C11	VSS_211	K29
AF6	VSS_032	AP14	C12	VSS_212	K33
AG36	VSS_033	AP17	C17	VSS_213	K35
AH2	VSS_034	AP22	C20	VSS_214	K37
AH3	VSS_035	AP25	C23	VSS_215	K39
AH33	VSS_036	AP27	C26	VSS_216	K5
AH36	VSS_037	AP30	C29	VSS_217	K6
AH37	VSS_038	AP36	C32	VSS_218	L10
AH38	VSS_039	AP37	C35	VSS_219	L17
AH39	VSS_040	AP4	C7	VSS_220	L20
AH40	VSS_041	AP40	C8	VSS_221	L23
AH5	VSS_042	AP5	D17	VSS_222	L26
AH8	VSS_043	AR11	D2	VSS_223	L29
AJ12	VSS_044	AR14	D20	VSS_224	L8
AJ15	VSS_045	AR17	D23	VSS_225	M1
AJ18	VSS_046	AR18	D26	VSS_226	M17
AJ21	VSS_047	AR19	D29	VSS_227	M2
AJ25	VSS_048	AR27	D32	VSS_228	M20
AJ27	VSS_049	AR30	D37	VSS_229	M23
AJ36	VSS_050	AR36	D39	VSS_230	M26
AJ5	VSS_051	AR5	D4	VSS_231	M29
AK1	VSS_052	AT1	D5	VSS_232	M33
AK10	VSS_053	AT10	D9	VSS_233	M35
AK13	VSS_054	AT12	E11	VSS_234	M37
AK14	VSS_055	AT13	E12	VSS_235	M39
AK16	VSS_056	AT15	E17	VSS_236	M5
AK22	VSS_057	AT16	E20	VSS_237	M6
AK28	VSS_058	AT17	E23	VSS_238	M9
AK31	VSS_059	AT2	E26	VSS_239	N8
AK32	VSS_060	AT25	E29	VSS_240	P1
AK33	VSS_061	AT27	E32	VSS_241	P2
AK34	VSS_062	AT28	E36	VSS_242	P36
AK35	VSS_063	AT29	E7	VSS_243	P38
AK36	VSS_064	AT3	E8	VSS_244	P40
AK37	VSS_065	AT30	F1	VSS_245	P5
AK4	VSS_066	AT31	F10	VSS_246	P6
AK40	VSS_067	AT32	F13	VSS_247	P33
AK5	VSS_068	AT33	F14	VSS_248	P35
AK6	VSS_069	AT34	F17	VSS_249	P37
AK7	VSS_070	AT35	F2	VSS_250	P39
AK8	VSS_071	AT36	F20	VSS_251	R8
AK9	VSS_072	AT37	F23	VSS_252	T1
AL11	VSS_073	AT38	F26	VSS_253	T5
AL14	VSS_074	AT39	F29	VSS_254	T6
AL17	VSS_075	AT4	F35	VSS_255	U8
AL19	VSS_076	AT40	F37	VSS_256	V1
AL24	VSS_077	AT5	F39	VSS_257	V2
AL27	VSS_078	AT6	F5	VSS_258	V33
AL30	VSS_079	AT7	F6	VSS_259	V34
AL36	VSS_080	AT8	F9	VSS_260	V35
AL5	VSS_081	AT9	G11	VSS_261	V36
AM1	VSS_082	AU1	G12	VSS_262	V37
AM11	VSS_083	AU26	G17	VSS_263	V38
AM14	VSS_084	AU34	G20	VSS_264	V39
AM17	VSS_085	AU4	G23	VSS_265	V40
AM2	VSS_086	AU6	G26	VSS_266	V5
AM21	VSS_087	AU8	G29	VSS_267	W6
AM23	VSS_088	AV10	G34	VSS_268	Y5
AM25	VSS_089		G7	VSS_269	Y8
	VSS_090			VSS_270	
A4	VSS_NCTF_01		AY37	VSS_NCTF_03	
AV39	VSS_NCTF_02		B3	VSS_NCTF_04	



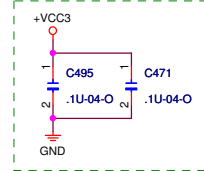
www.aitech1.ru

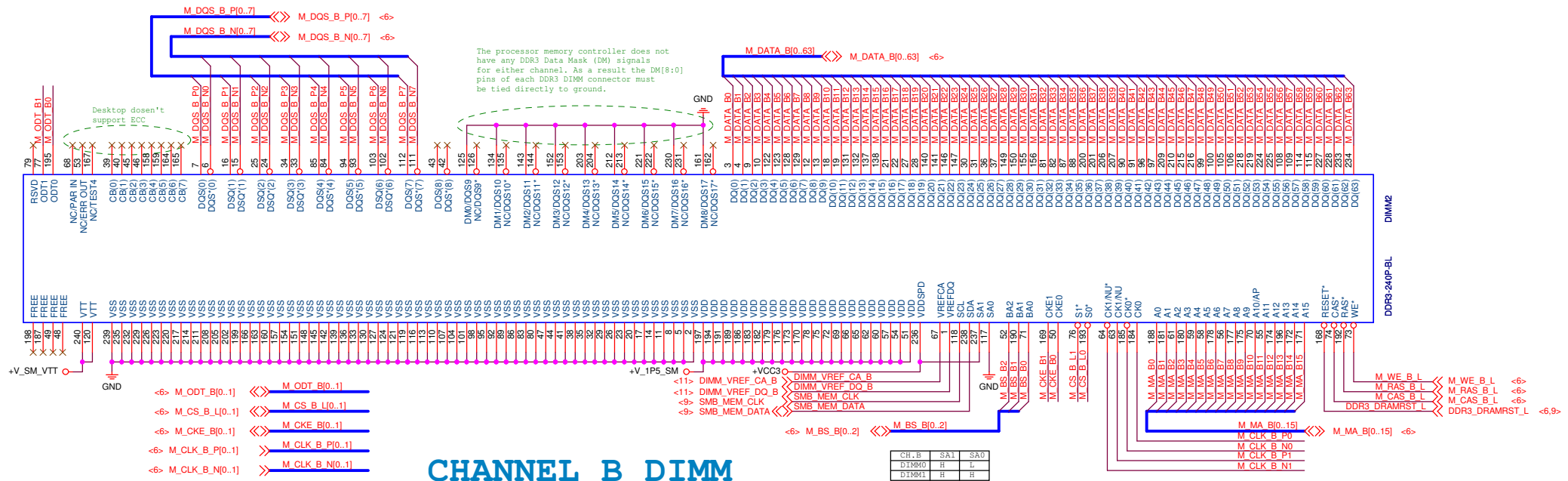


For CHANNEL A DIMM1



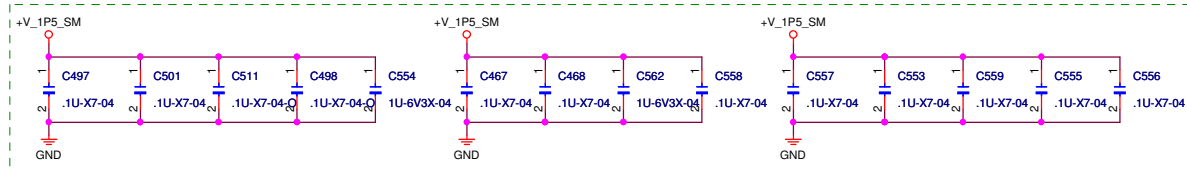
PLACE BETWEEN CHA & CHB.
DO NOT PUNCH VIA.



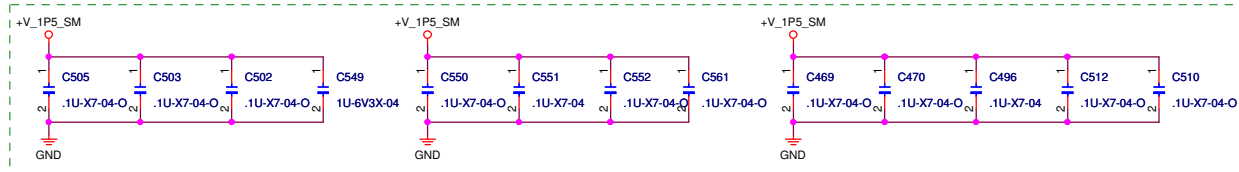


CHANNEL B DIMM

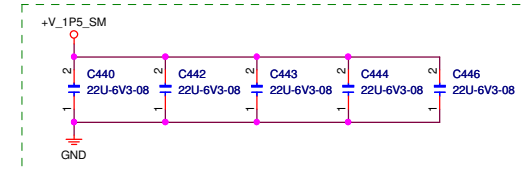
www.aitech1.ru



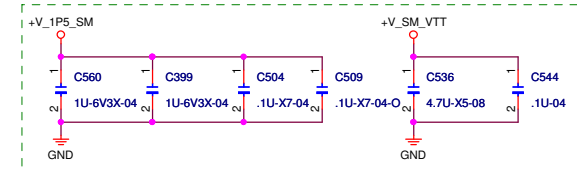
STITCHING CAPS FOR CMD, ADDR, CTL.BETWEEN CH1 & CH2.



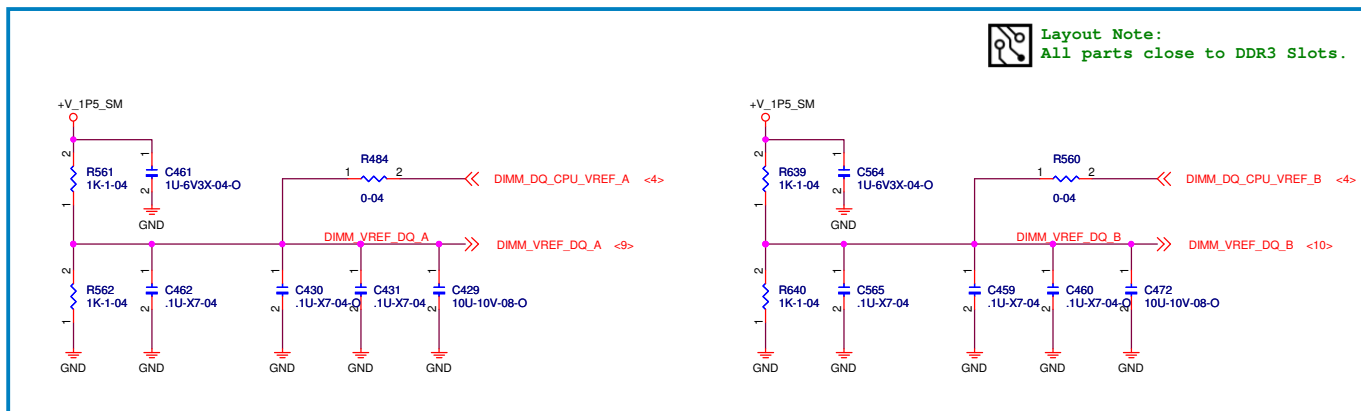
STITCHING CAPS FOR CMD, ADDR, CTL.BETWEEN CH1 & CH2.



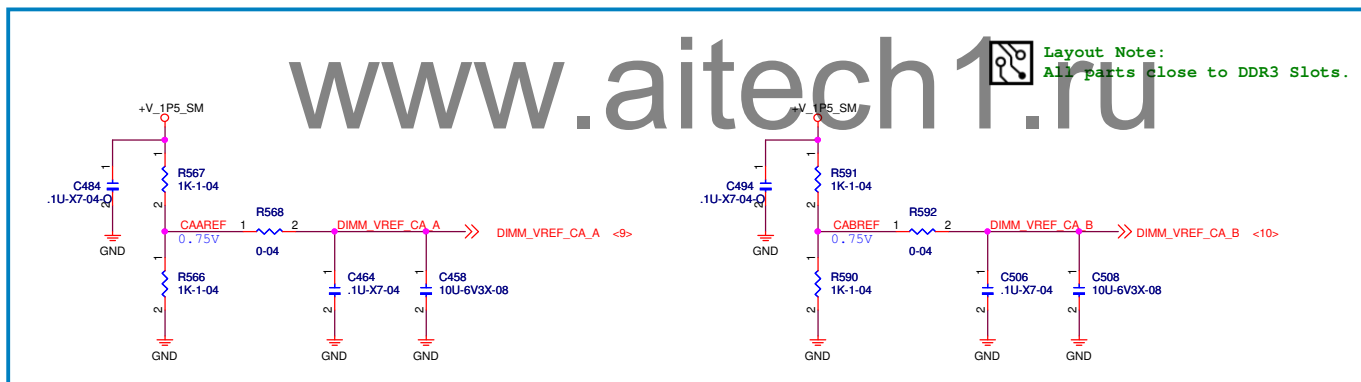
Match PDG_V1.5 requirement, Intel recommend MLCC for Vdim power.



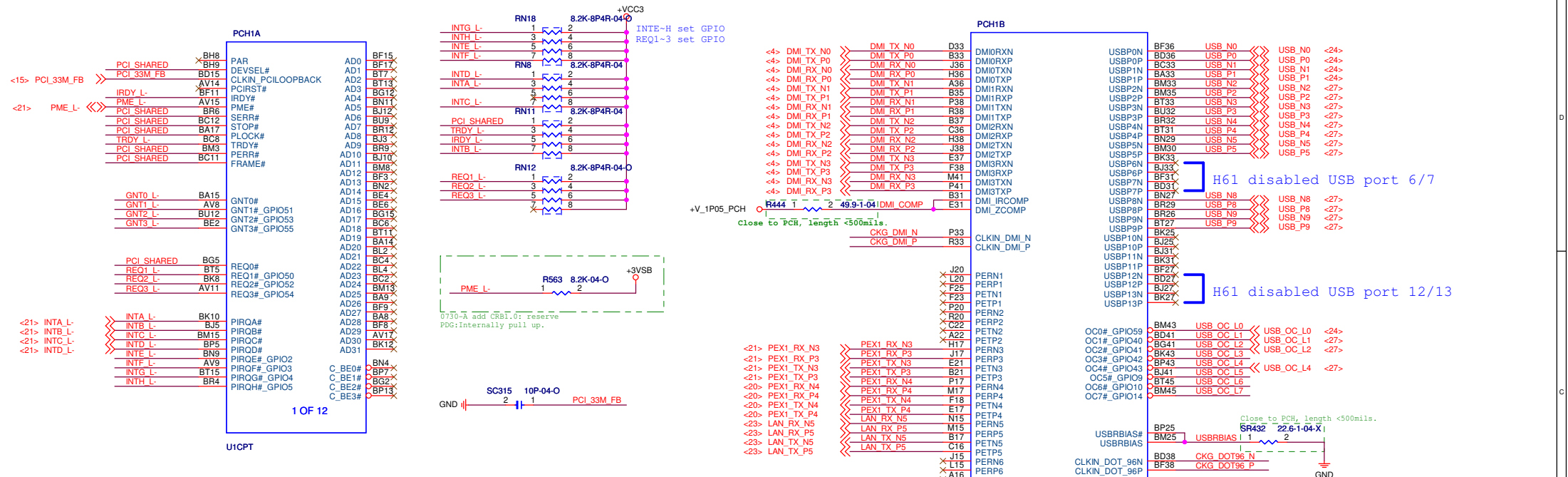
For CH1 & CH2.



DIMM_VREF_DQ Control Circuit



DIMM_VREF_CA Circuit



Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

* GNT1[0..3]#
GPIO19 have been internal pull high to +VCC3

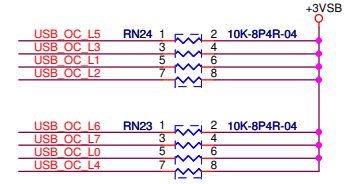
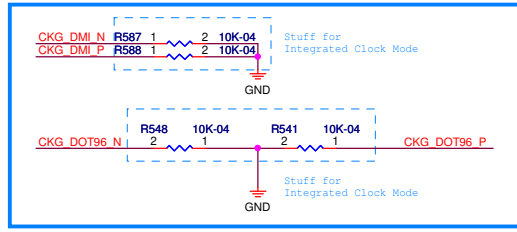
<13> GPIO19 >>> GPIO19 1 2 10K-04
GNT1_L 1 2 4.7K-04-0
Reserve for Driving.

+VCC3

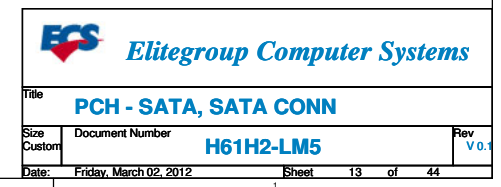
GND

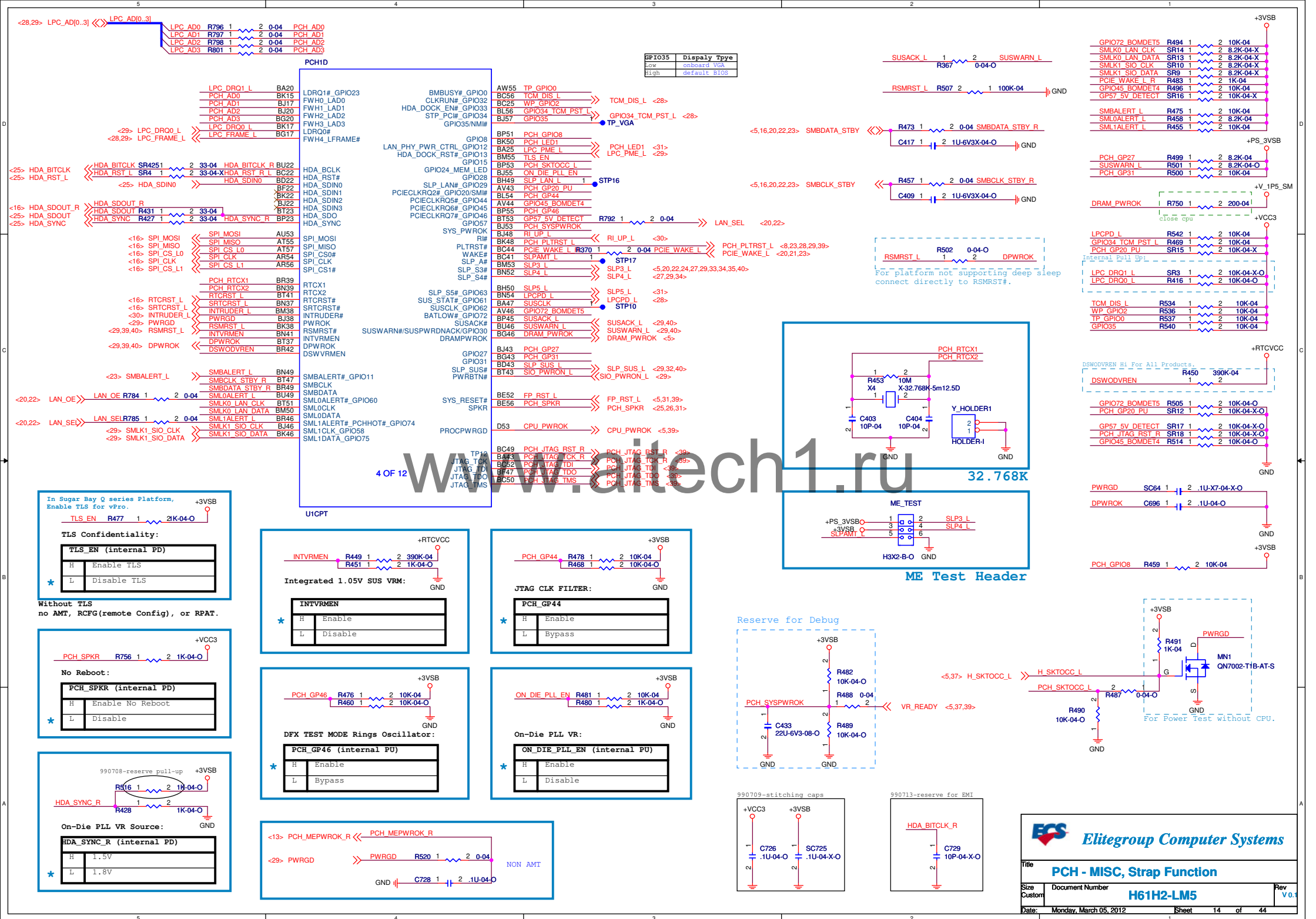
R509 1K-04-0 1 2 GPIO19
R393 1K-04-0 1 2 GNT0_L
R392 1K-04-0 1 2 GNT1_L
R410 1K-04-0 1 2 GNT2_L
R394 1K-04-0 1 2 GNT3_L

GPIO19: Boot Device Select Strap.
GNT0_L: No More Information in EDS V0.7
GNT1_L: Boot Device Select Strap.
GNT2_L: ESI Strap (Server Only), DON'T Pull Low in Desktop.
GNT3_L: Top-Block Swap Override Mode, When Sampled Low.



www.aitech.ru

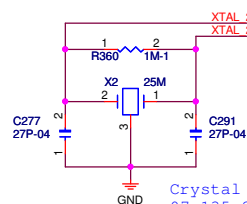






Layout Note:
PCI Clock Max 15000MILS

<29> SIO48M << SIO48M R376 1 2 22-04 SIO48M R
PDG 0.7 33 Q ± 5% for Single-End (except PCI Clocks)



Crystal P/N:
07-135-250035
07-135-250036

PCH1H

CLKOUT_PCH0
CLKOUT_PCH1
CLKOUT_PCH2
CLKOUT_PCH3
CLKOUT_PCH0LOOPBACK
CLKOUTFLEX0_GPIO64
CLKOUTFLEX1_GPIO65
CLKOUTFLEX2_GPIO66
CLKOUTFLEX3_GPIO67

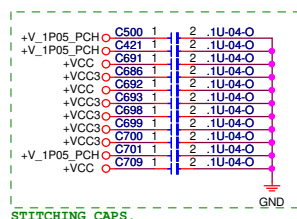
XCLK_RCOMP
REFCLK14IN

XTAL25_OUT
XTAL25_IN

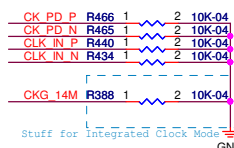
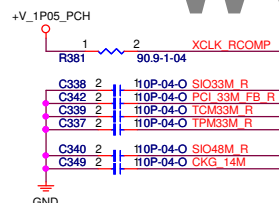
8 of 12

UICPT

CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_GND0_N
CLKIN_GND0_P
CLKOUT_ITPXPDP_N
CLKOUT_ITPXPDP_P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLKOUT_PCIE2N
CLKOUT_PCIE2P
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
R27 CLK IN N
P27 CLK IN P
W53 CK PD N
V52 CK PD P
R52 XDP CPU CLK DN
N52 XDP CPU CLK DP
AE2 XDP PCH CLK DN
AF1 XDP PCH CLK DP
P31 CK CPU 100M N
R31 CK CPU 100M P
N56
M55
AE6
AC6
AA5
W5
AB12 GLAN CLK N
AB14 GLAN CLK P
AB9
AB8
Y9 BRIDGE CLK N
Y8 BRIDGE CLK P
AF3 PEX1_A_100M N
AG2 PEX1_A_100M P
AB3
AA2
AG8 PEX16_100M N
AG9 PEX16_100M P
AE12
AE1



STITCHING CAPS.



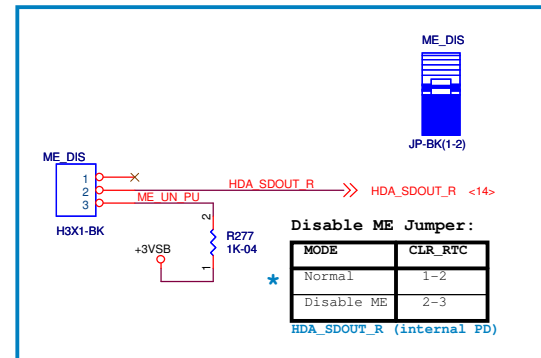
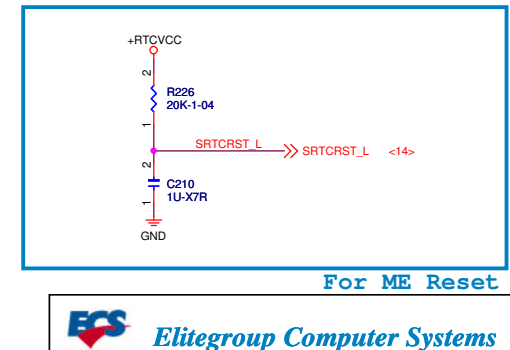
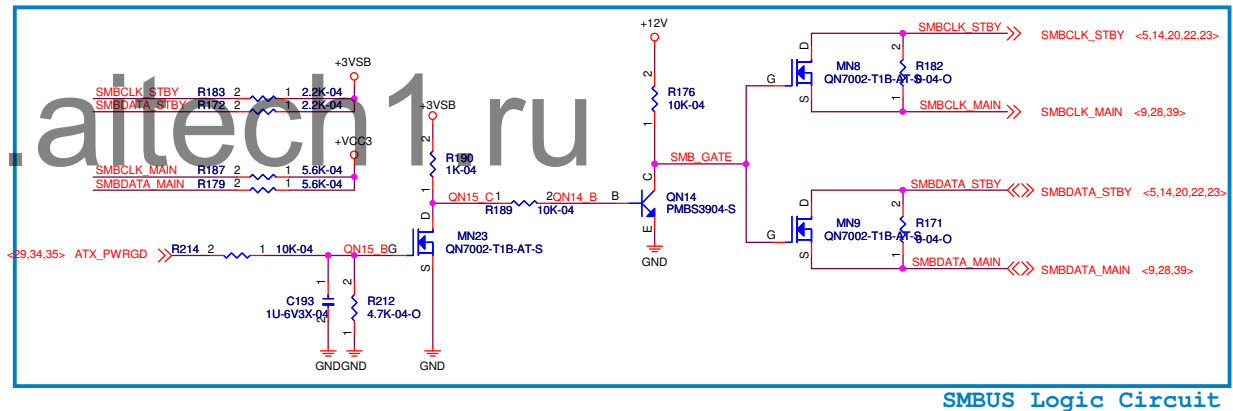
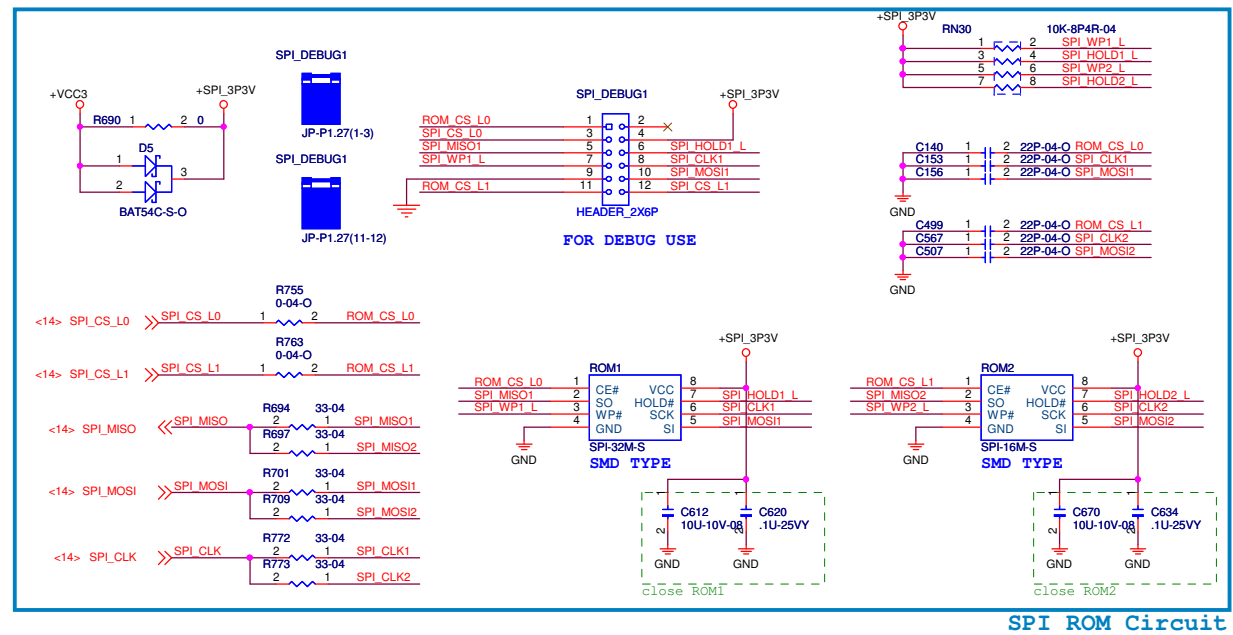
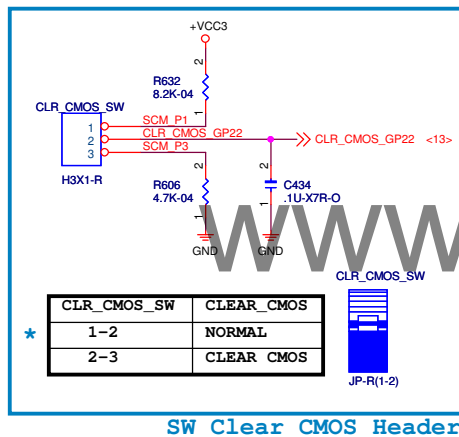
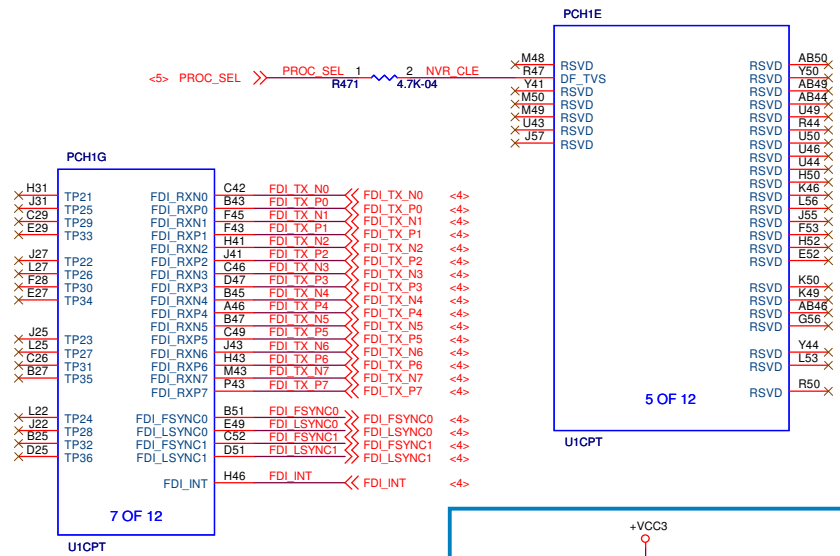
Stuff for Integrated Clock Mode

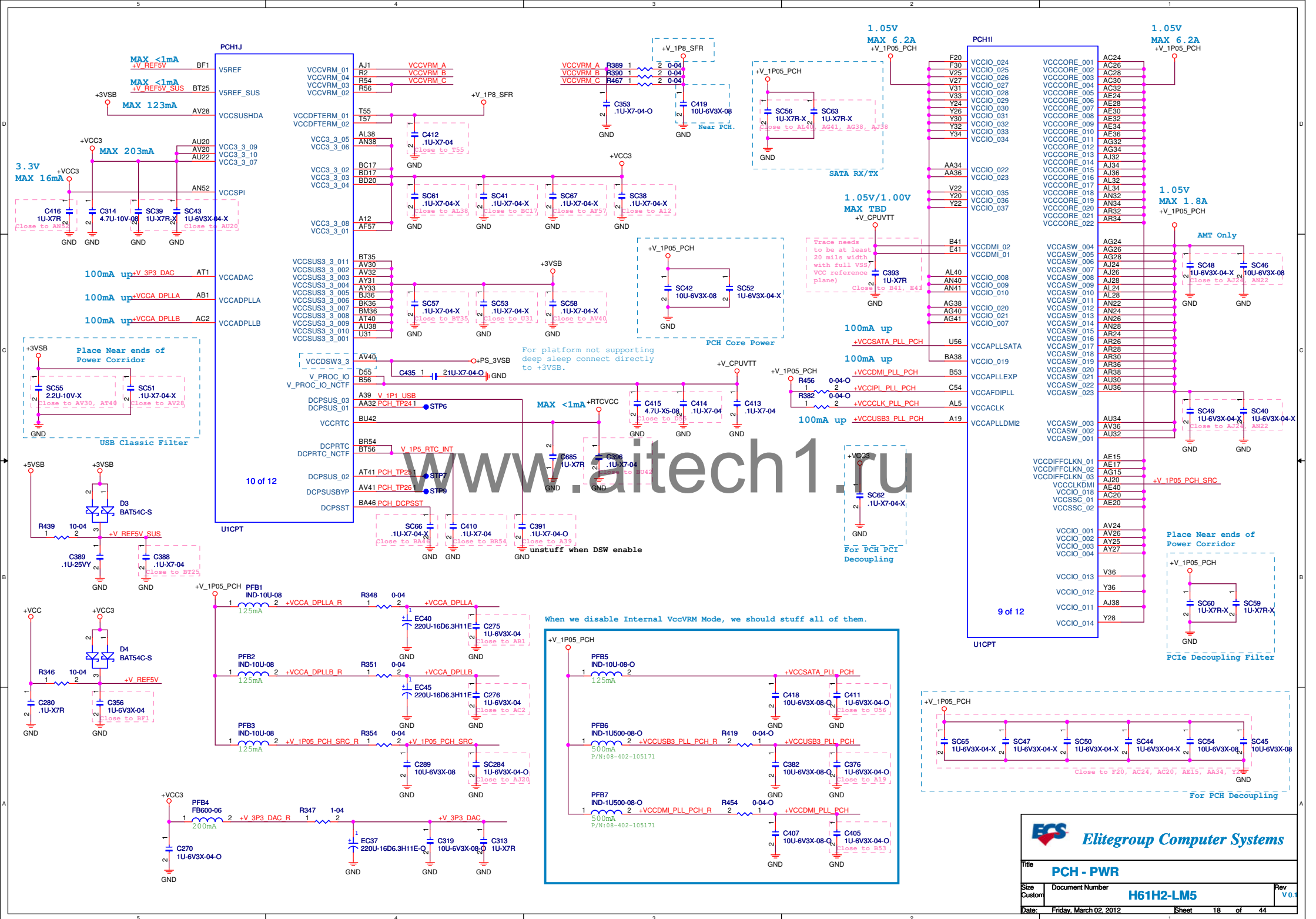
www.aitech1.ru

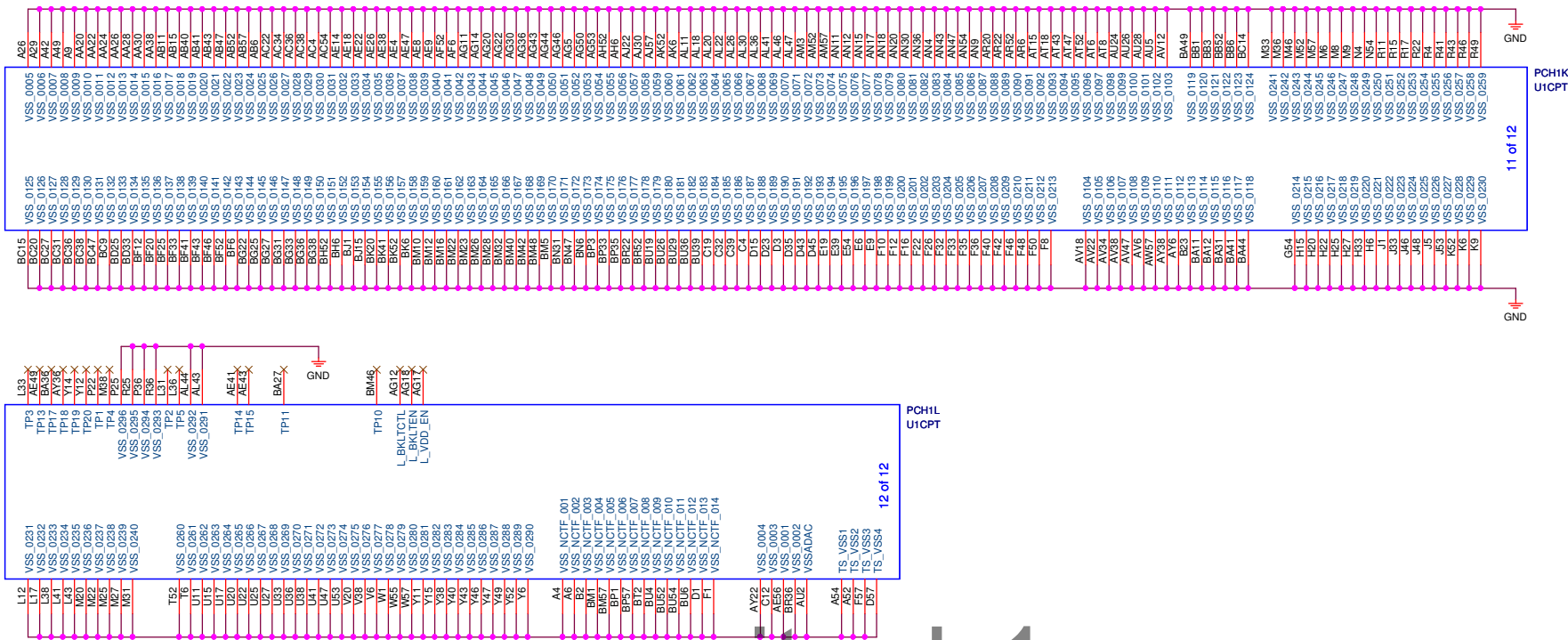


Elitegroup Computer Systems

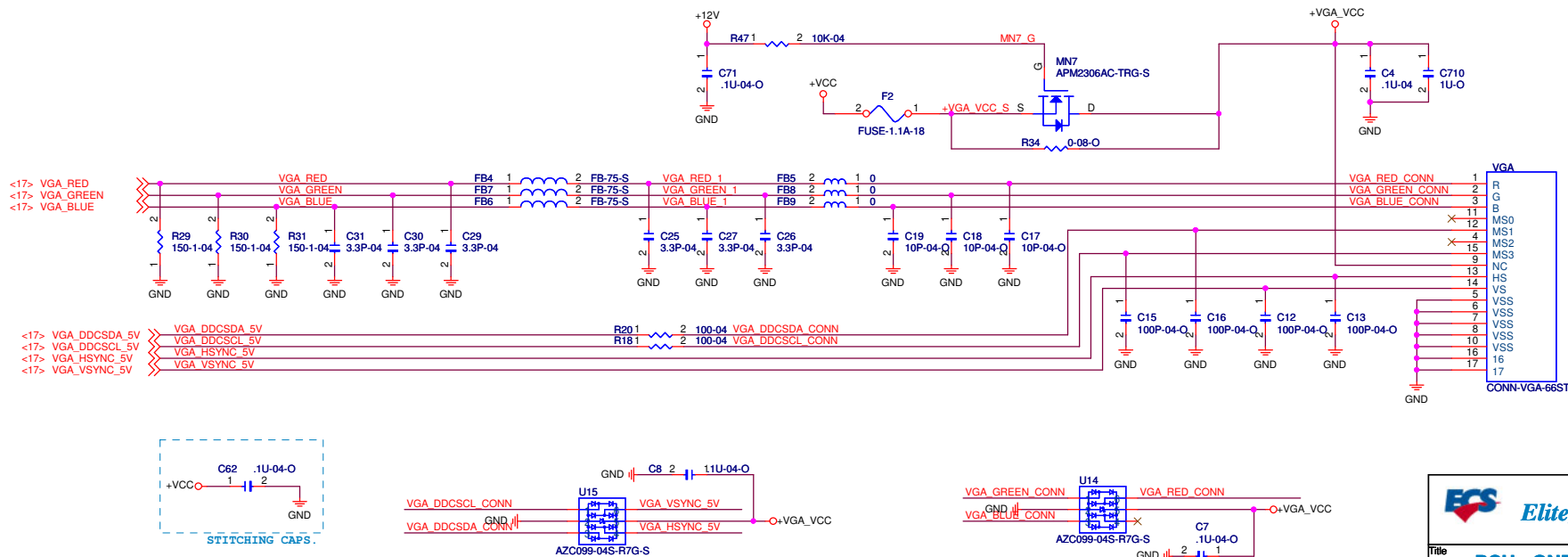
Title			PCH - CLK IO
Size	Document Number	H61H2-LM5	
Custom		Rev	V0.1
Date:	Friday, March 02, 2012	Sheet	15 of 44





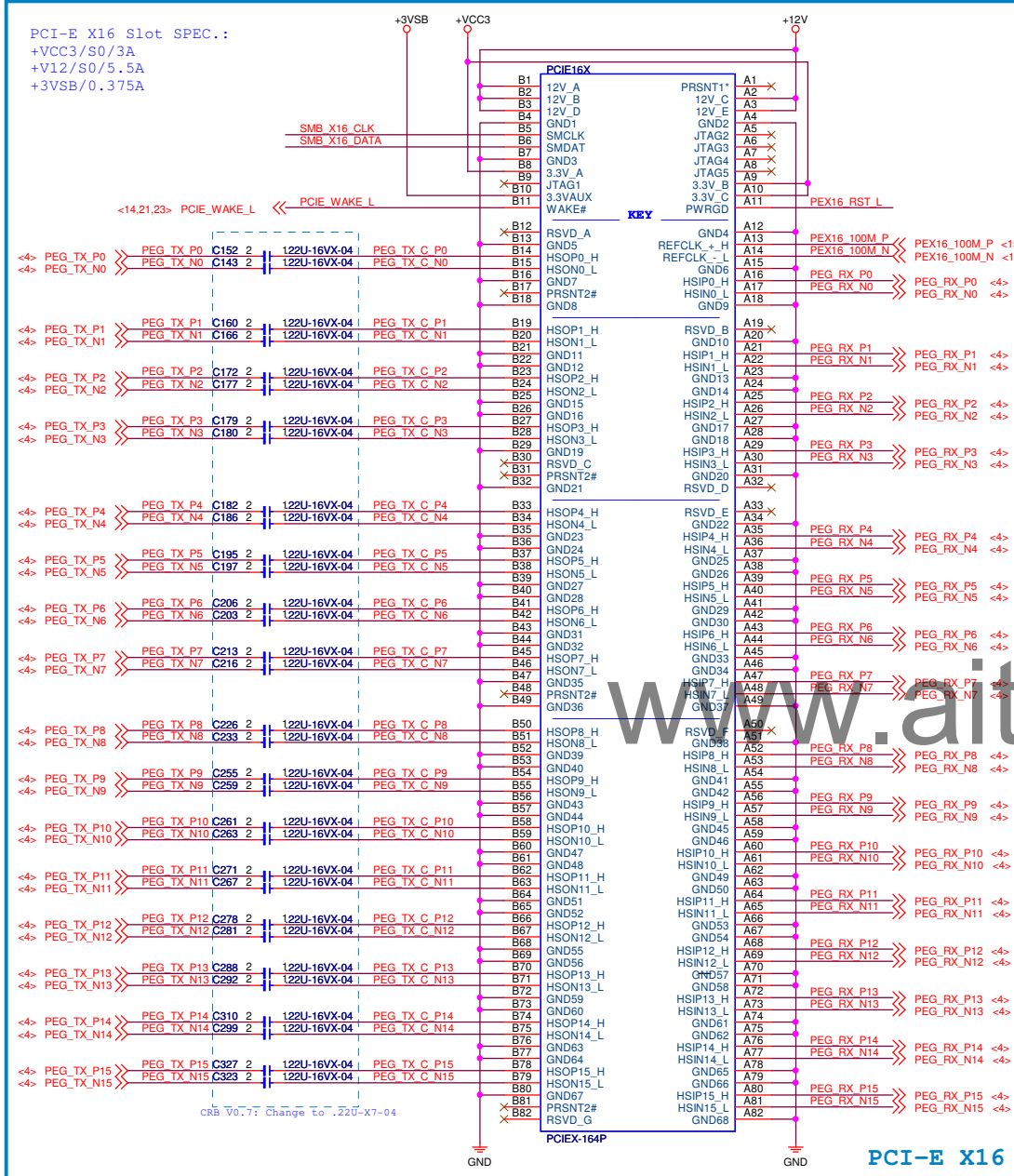


www.aitech1.ru



PCI-E X16 Slot SPEC.:

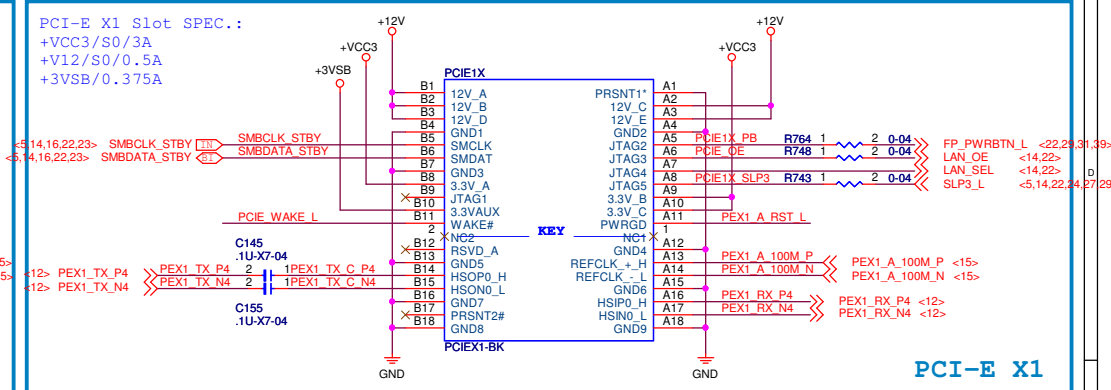
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A



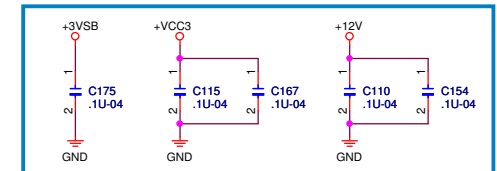
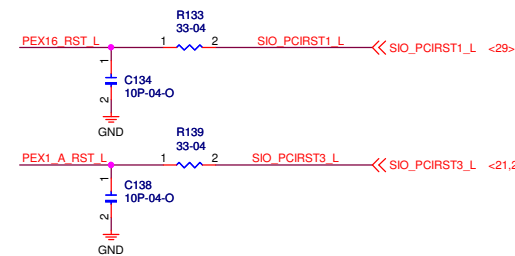
PCI-E X16

PCI-E X1 Slot SPEC.:

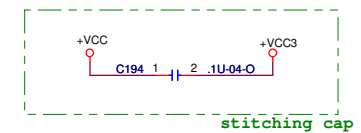
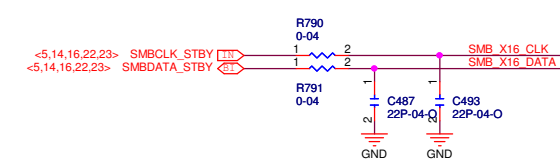
+VCC3/S0/3A
+V12/S0/0.5A
+3VSB/0.375A



PCI-E X1



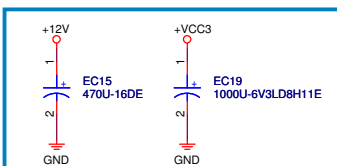
PCI-E X1 Decoupling Cap.



stitching cap

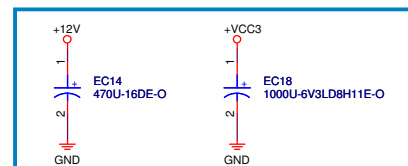
PCIE*16,PCIE*1 Slot	
Title	Document Number
Size Custom	H61H2-LM5
Date: Friday, March 02, 2012	Sheet 20 of 44

04-711-102073
E/C.1000uF.16V.20%...105C.RT D10*17mm

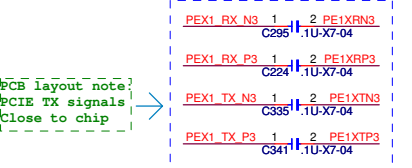
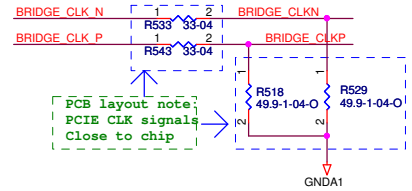
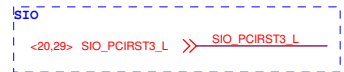
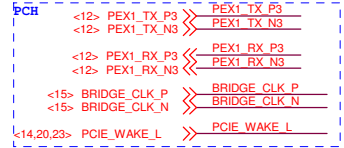
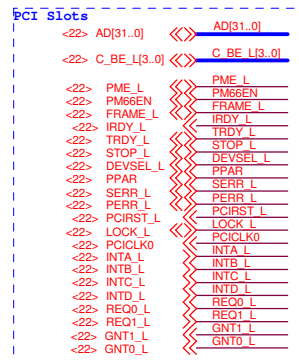


Between PEX16 & PEX1_1

04-711-102073
E/C.1000uF.16V.20%...105C.RT D10*17mm



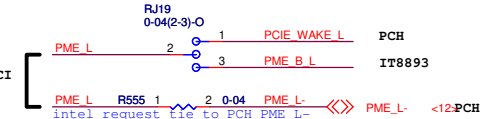
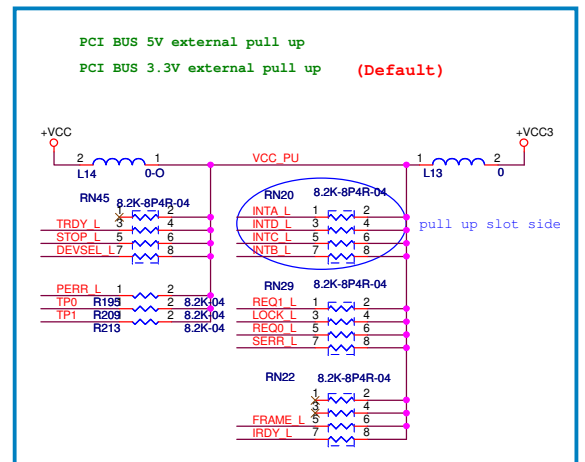
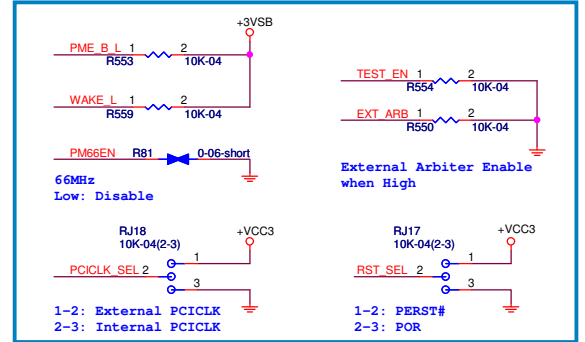
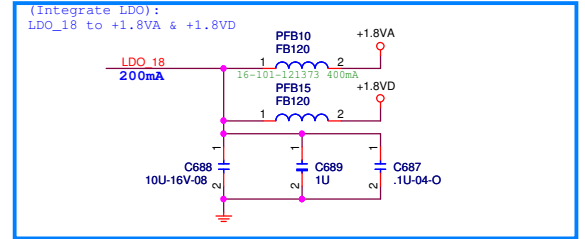
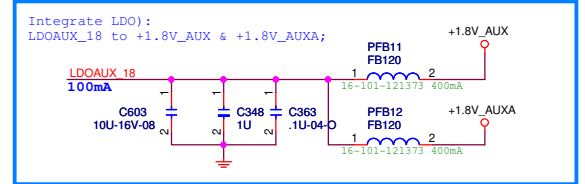
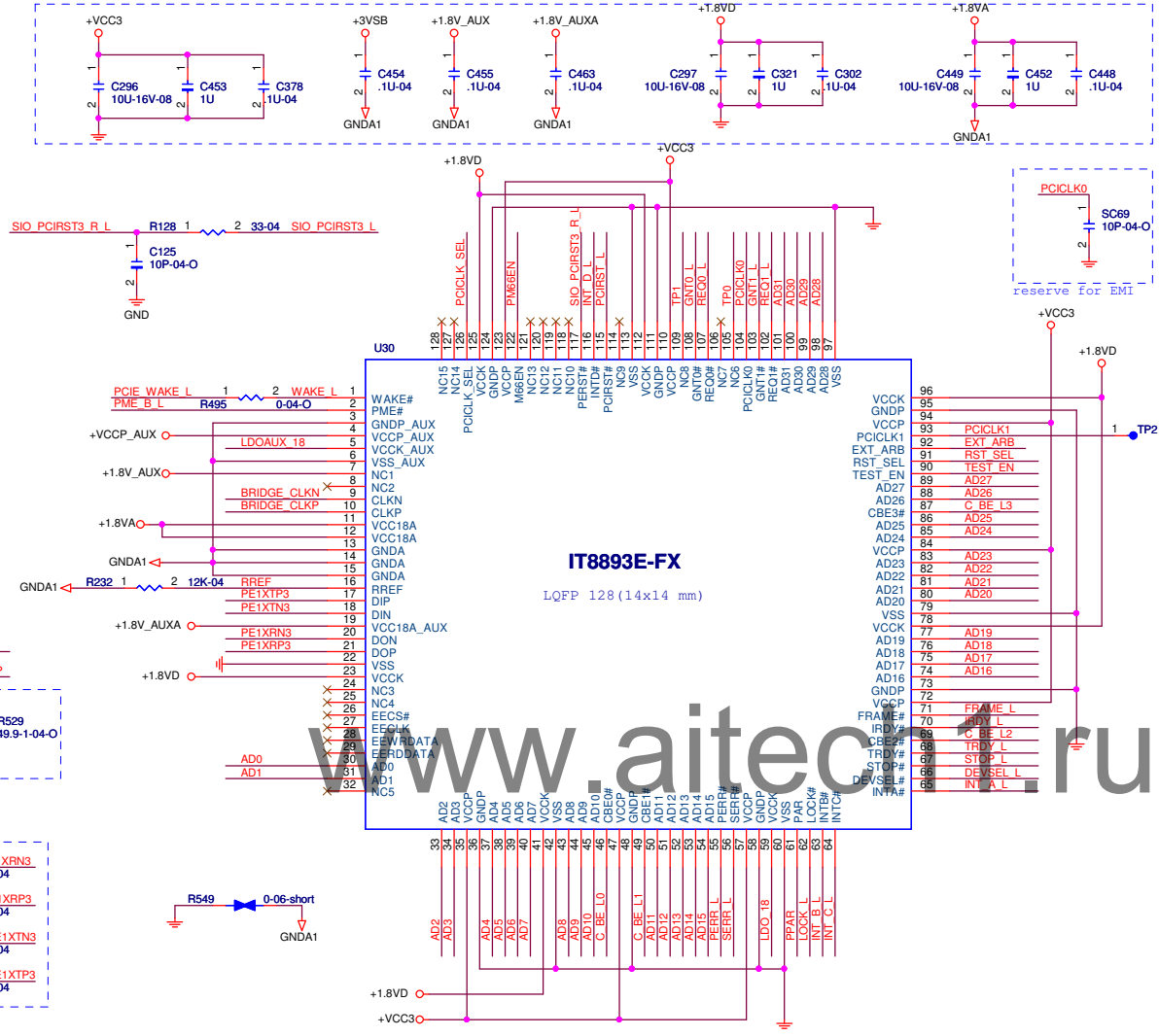
Between PEX1_1 & PCI1



LDOAUX_18: 1.8V LDO output with max 100mA;
LDO_18: 1.8V LDO output with max 200mA;
+1.8VA: Analog Transceiver PWR of PHY;
+V_LPB_SFR: 1.8V Core Power
+1.8V_AUX: 1.8V AUX PWR for Core
+1.8V_AUXA: 1.8V Analog AUX PWR for AUX PWR

PCIE CLK PCB layout note:
To meet Differential Impedance :100 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
CLKP and CLKN trace width:7 mils
Space between CLKP and CLKN:14 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 4 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inches (Max.)
The size of R4;R5 is "0402"
The size of R6;R7 is "0402"

PCIE DIP;DIN;DOP;DON PCB layout note:
To meet Differential Impedance :85 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
PCIE DIP and DIN trace width:9.5 mils
PCIE DOP and DON trace width:9.5 mils
Space between DIP/DIN and DOP/DON:14.5 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 2 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inches (Max.)
The size of C24;C25 is "0402"



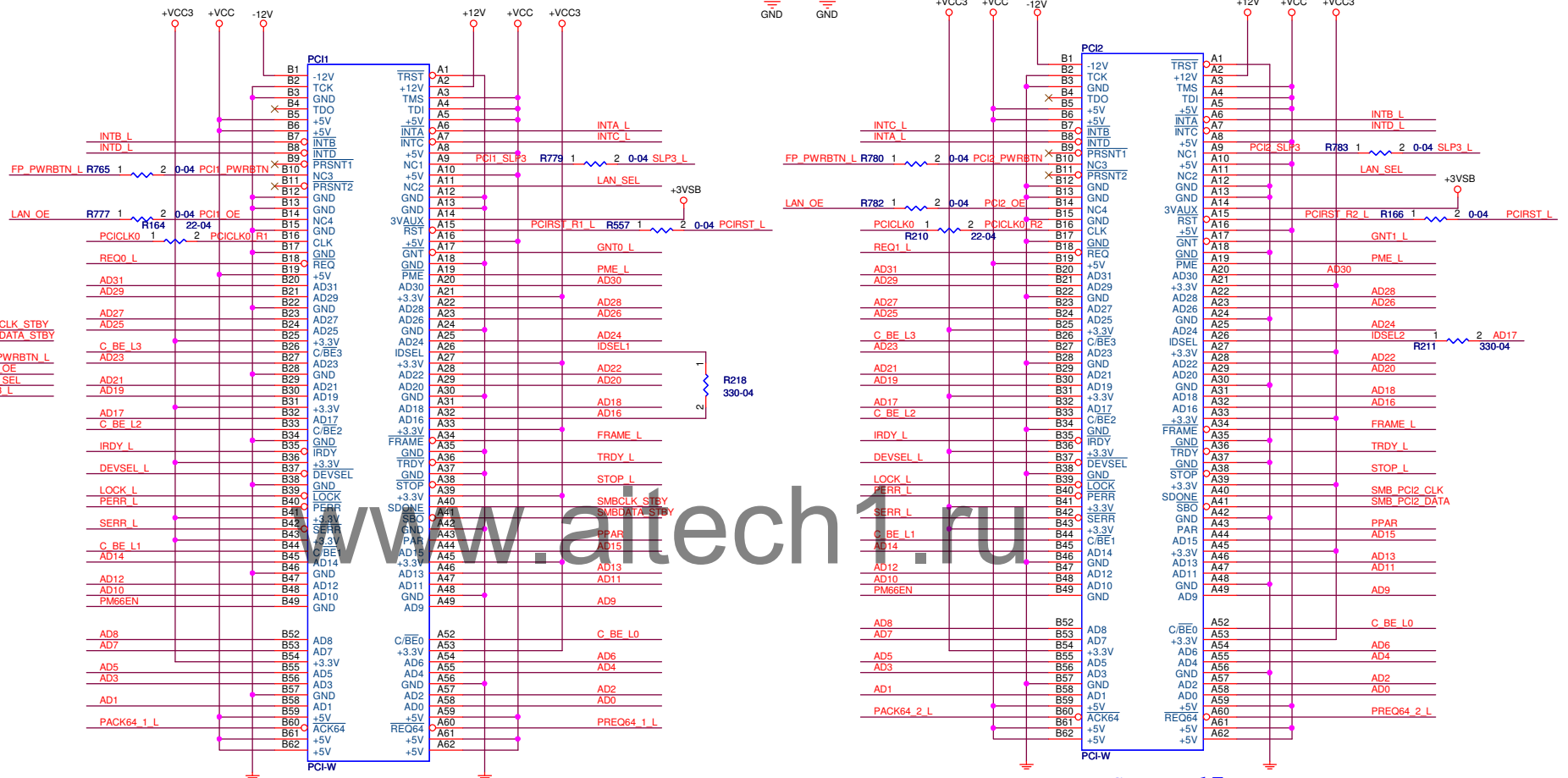
PCI BUS

<21> AD[31..0]	<>>	AD[31..0]
<21> C_BE_L[3..0]	<>>	C_BE_L[3..0]
<21> GNT0_L	<>>	GNT0_L
<21> GNT1_L	<>>	GNT1_L
<21> REQ0_L	<>>	REQ0_L
<21> REQ1_L	<>>	REQ1_L
<21> INTA_L	<>>	INTA_L
<21> INTB_L	<>>	INTB_L
<21> INTC_L	<>>	INTC_L
<21> INTD_L	<>>	INTD_L
<21> PPAR	<>>	PPAR
<21> DEVSEL_L	<>>	DEVSEL_L
<21> IRDY_L	<>>	IRDY_L
<21> PME_L	<>>	PME_L
<21> SERR_L	<>>	SERR_L
<21> STOP_L	<>>	STOP_L
<21> LOCK_L	<>>	LOCK_L
<21> TRDY_L	<>>	TRDY_L
<21> FERR_L	<>>	FERR_L
<21> FRAME_L	<>>	FRAME_L
<21> PCIRST_L	<>>	PCIRST_L
<21> PCICLK0	<>>	PCICLK0
<21> PM66EN	<>>	PM66EN

<5,14,16,20,23> SMBCLK_STBY	<>>	SMBCLK_STBY
<5,14,16,20,23> SMBDATA_STBY	<>>	SMBDATA_STBY
<20,29,31,39> FP_PWRBTN_L	<>>	FP_PWRBTN_L
<14,20> LAN_OE	<>>	LAN_OE
<14,20> LAN_SEL	<>>	LAN_SEL
<5,14,20,24,27,29,33,34,35,40> SLP3_L	<>>	SLP3_L

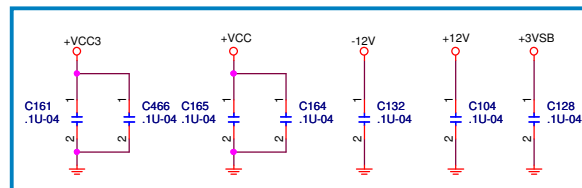
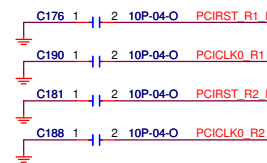
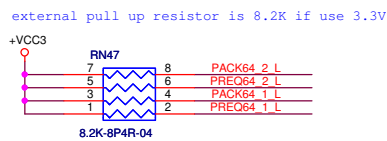
PCI Slot:
+VCC/S0/5A
+VCC3/S0/7.6A
+V12/S0/0.5A
+3VSB/0.375A

PCI Slot:
+VCC/S0/5A
+VCC3/S0/7.6A
+V12/S0/0.5A
+3VSB/0.375A

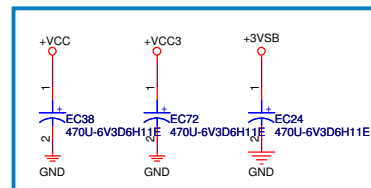


IDSEL=AD16
INT[A,B,C,D]
Legacy mode from PCH
INT[A,B,C,D]

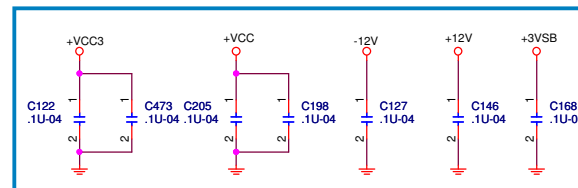
IDSEL=AD17
INT[B,C,D,A]
Legacy mode from PCH
INT[B,C,D,A]



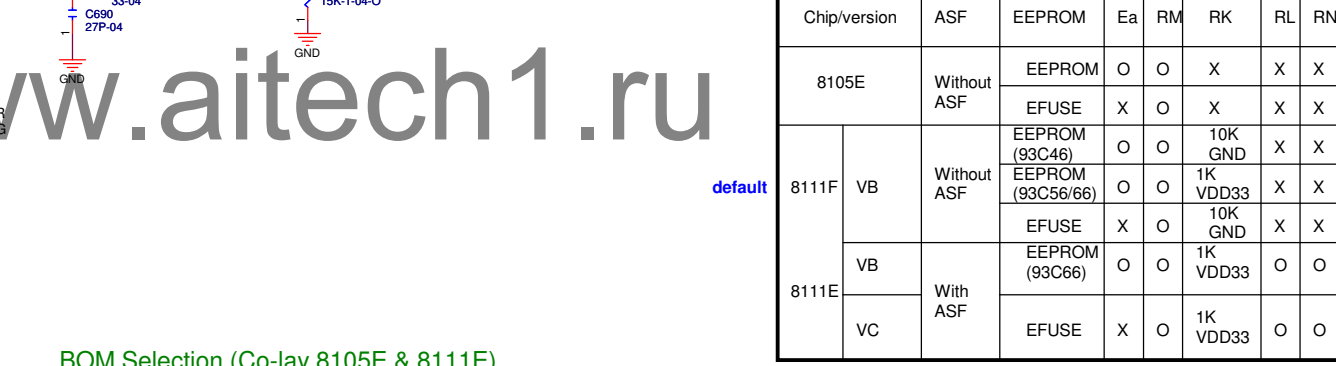
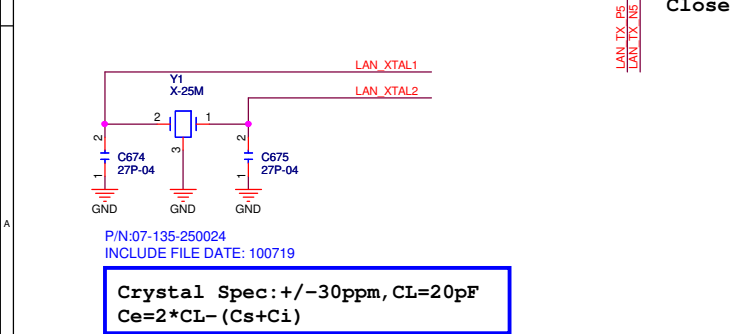
PCI1 Decoupling Cap.



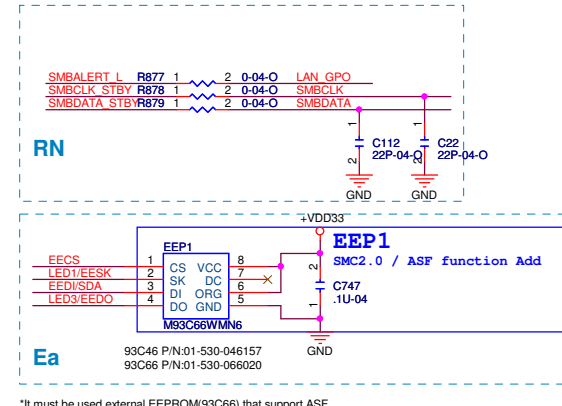
Between PCI1 & PCI2



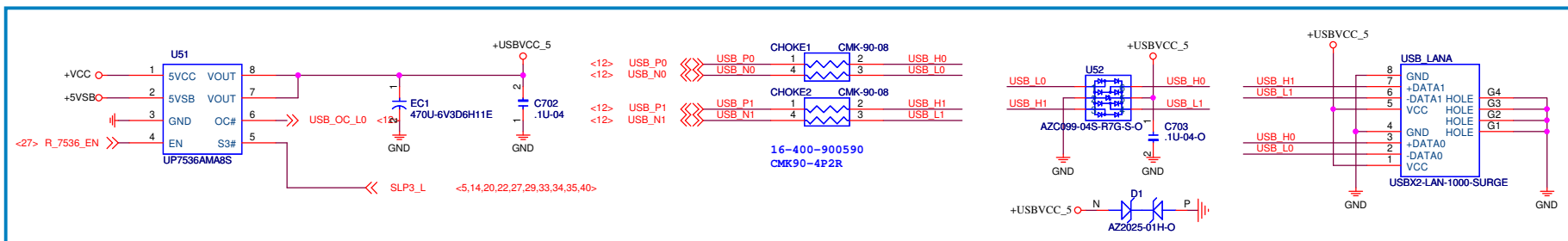
PCI2 Decoupling Cap.



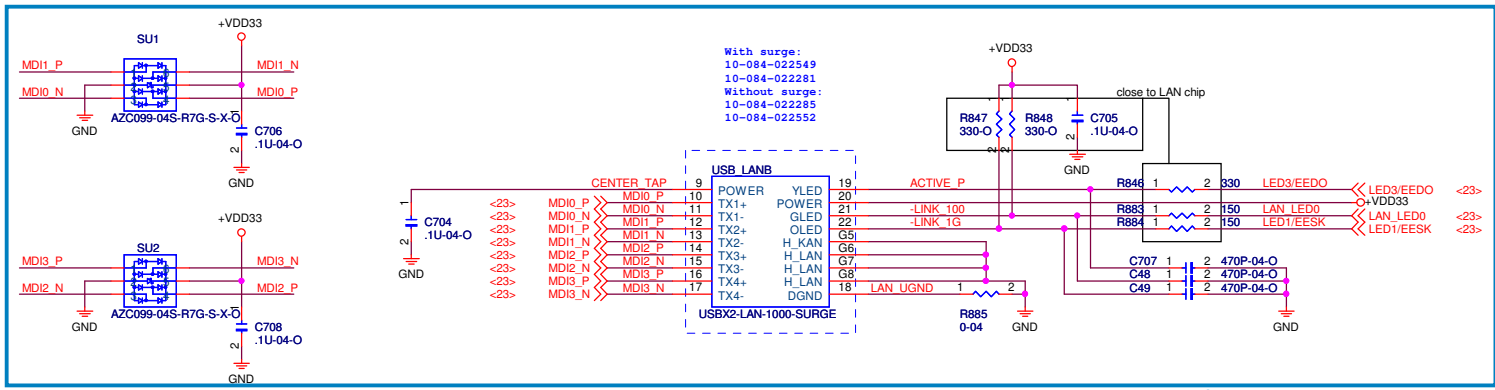
BOM Selection (Co-lay 8105E & 8111E)



*It must be used external EEPROM(93C66) that support ASF.



REAR SIDE 2 PORTS ON LANUSB CONN.



REAR SIDE 2 PORTS ON LANUSB CONN.

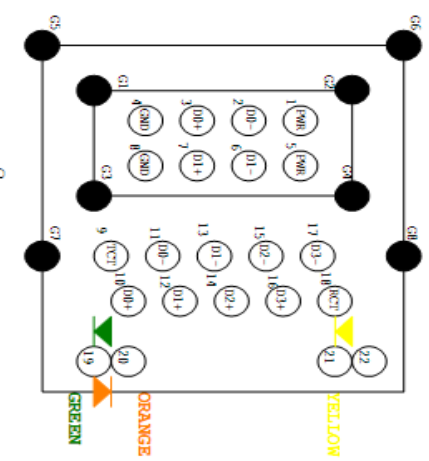
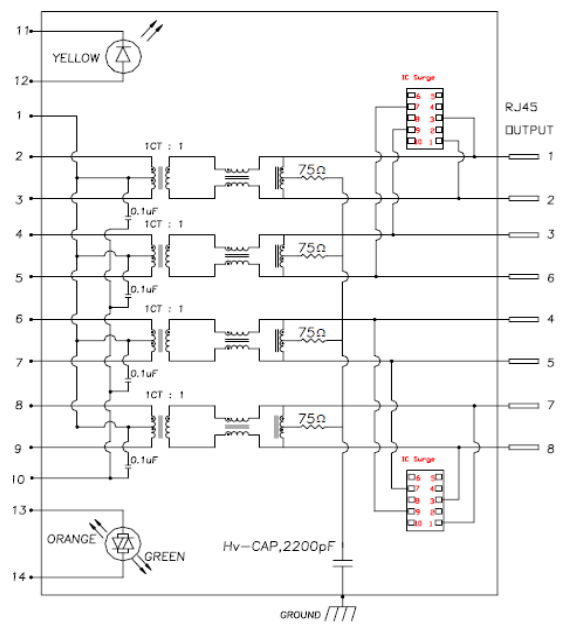
Place Caps between chipset and Lan connector in Bottom Side.

MDI0_P SC1 1 2 2.7P-04-X-O
MDI0_N SC2 1 2 2.7P-04-X-O
MDI1_P SC3 1 2 2.7P-04-X-O
MDI1_N SC4 1 2 2.7P-04-X-O
MDI2_P SC5 1 2 2.7P-04-X-O
MDI2_N SC6 1 2 2.7P-04-X-O
MDI3_P SC7 1 2 2.7P-04-X-O
MDI3_N SC8 1 2 2.7P-04-X-O

For EMI
EMI value must be tuned.

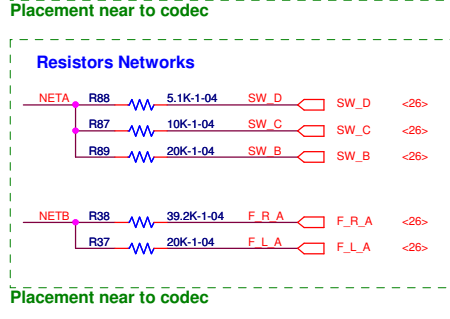
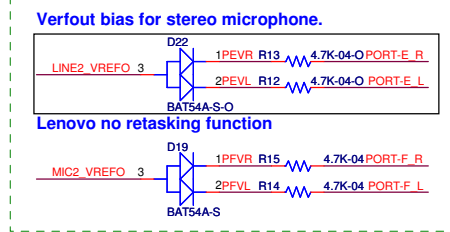
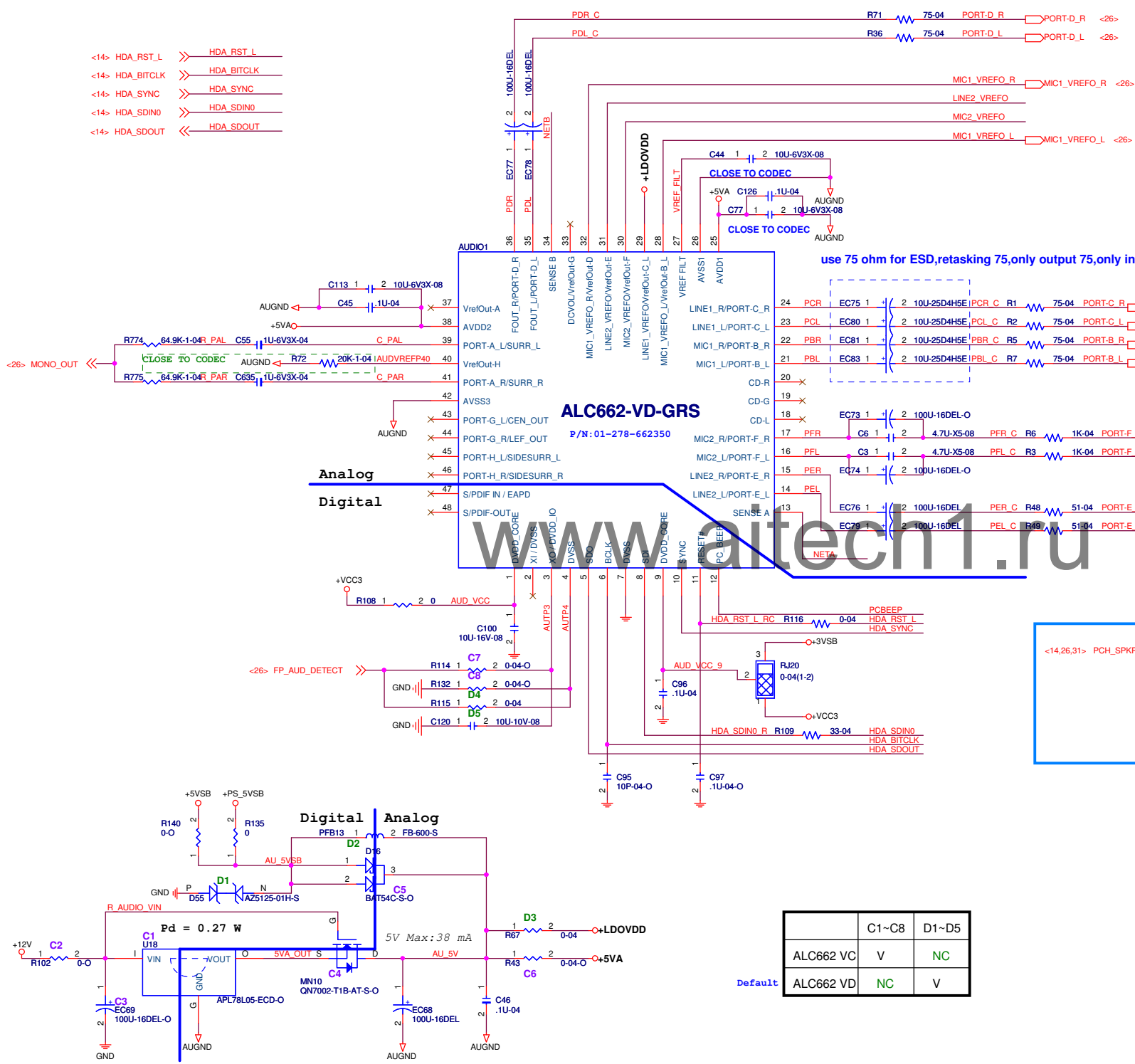


ESD for LAN LED



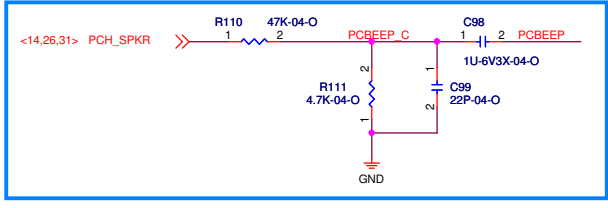
WOL	status	Yellow	Grn/Org
don't care	No Link	off	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off	off
on	10M,inactive		off
on	10M,active		off
on	100M,inactive		
on	100M,active		
on	1G,inactive		
on	1G,active		

always on
always on
always on
blinking

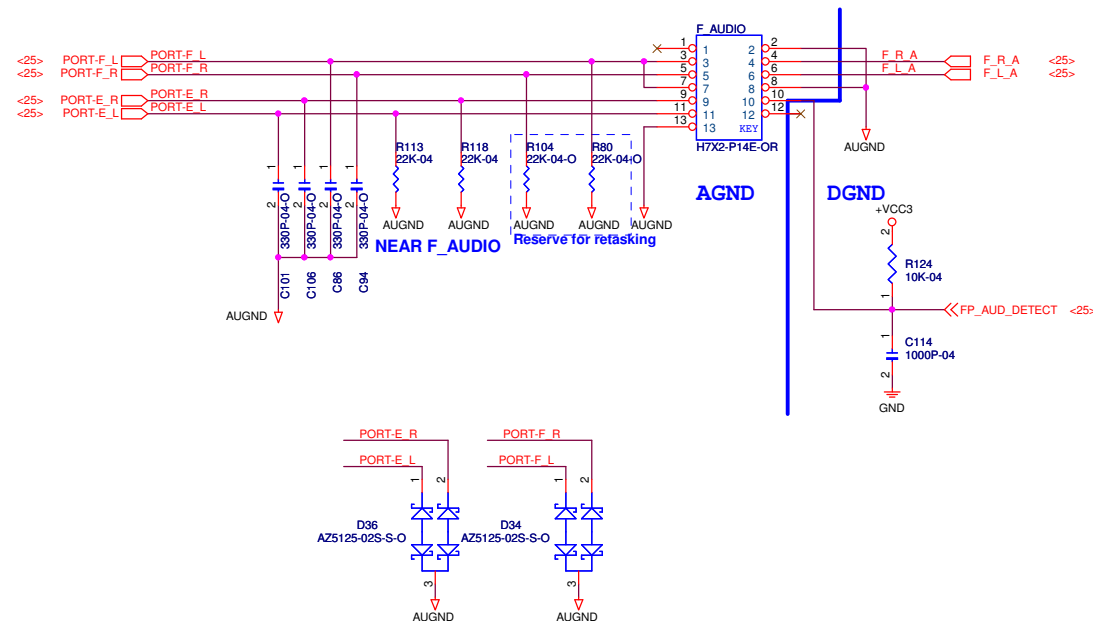
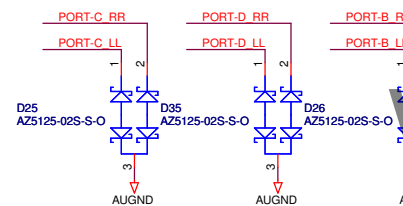
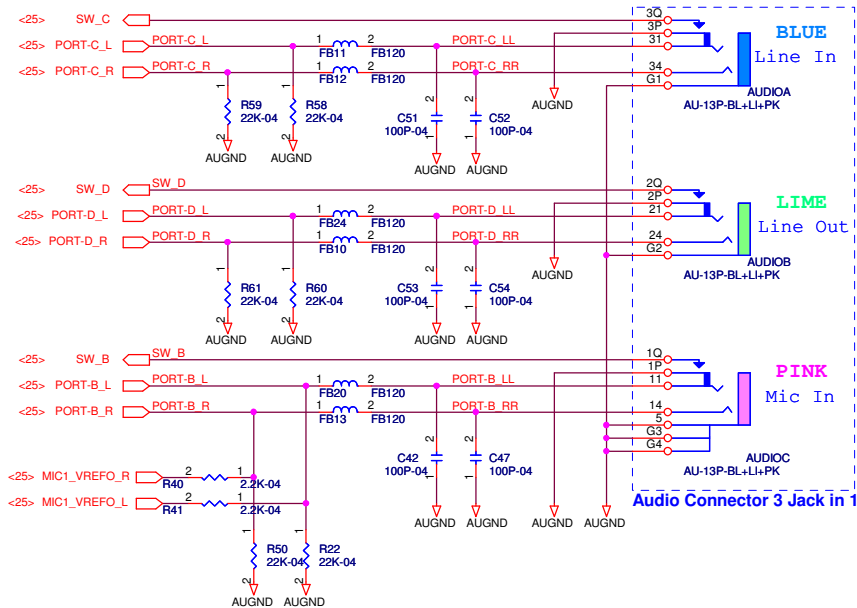


use 75 ohm for ESD, retasking 75, only output 75, only input 1K.

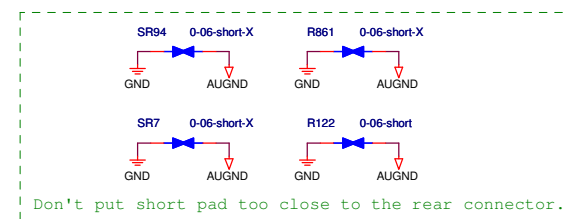
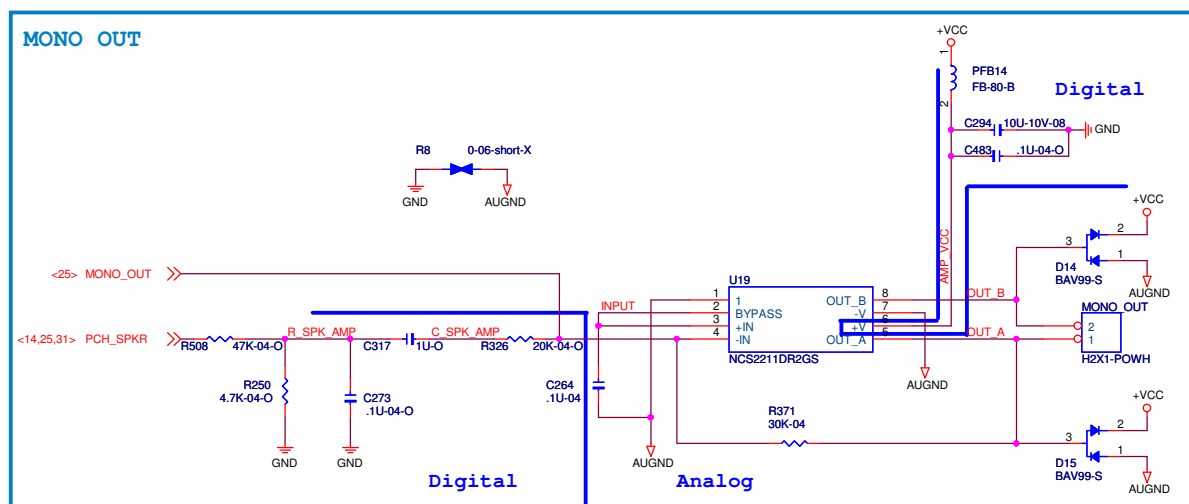
www.aitech1.ru



	C1~C8	D1~D5
ALC662 VC	V	NC
ALC662 VD	NC	V

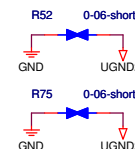


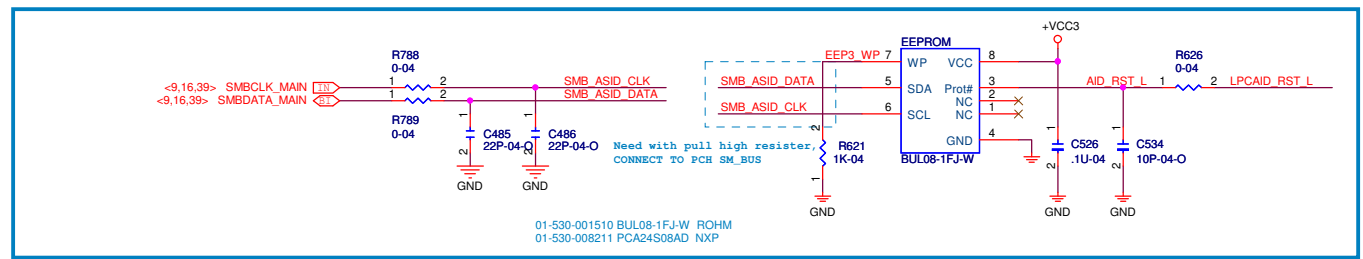
www.aitech1.ru



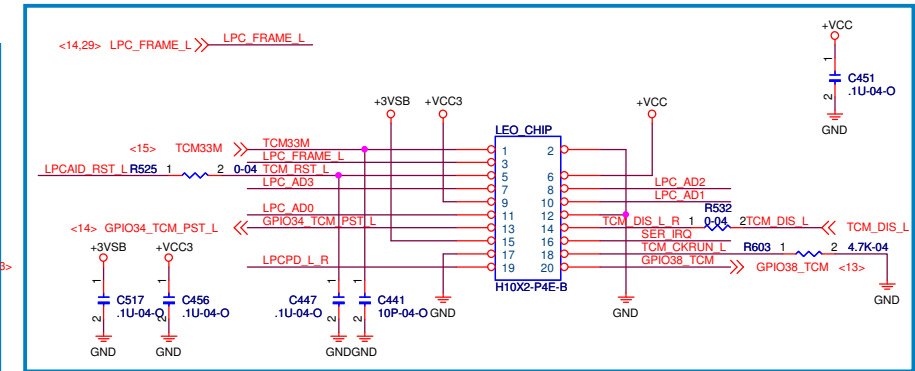


uP7536 Enable use	Level shift	RJA	RJB	S4/S5 USB_5V_DUAL	Customer
VDIMM	N A	0ohm (1-2)	N A	0 Volt	Lenovo S4/S5 w/o USB_5V_DUAL
VDIMM level shift (3.3V)	Stuff	0ohm (2-3)	N A	0 Volt	





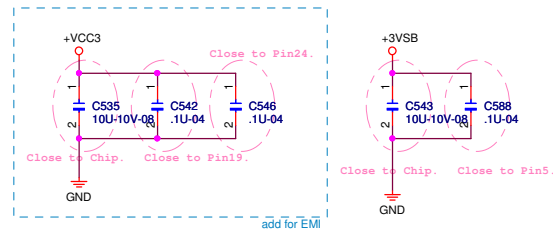
Asset ID Circuit



TCM Header Circuit

Layout Note:
LPC Routing: PCH->TCM->LPC_DEBUG->TPM (ONE WAY)

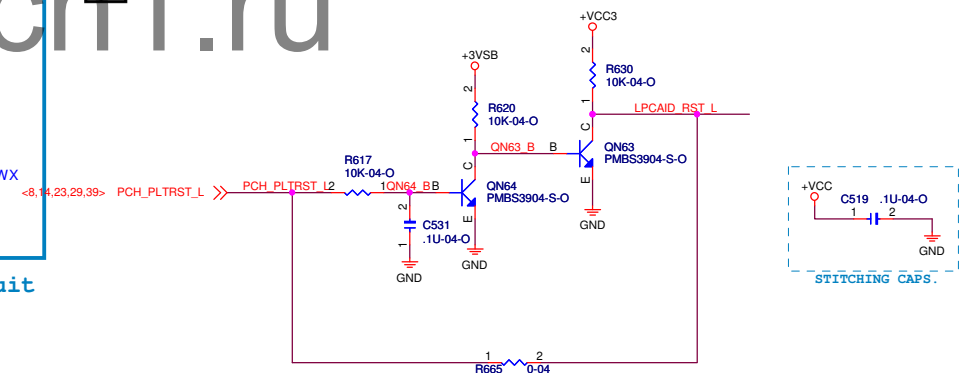
www.aitech1.ru



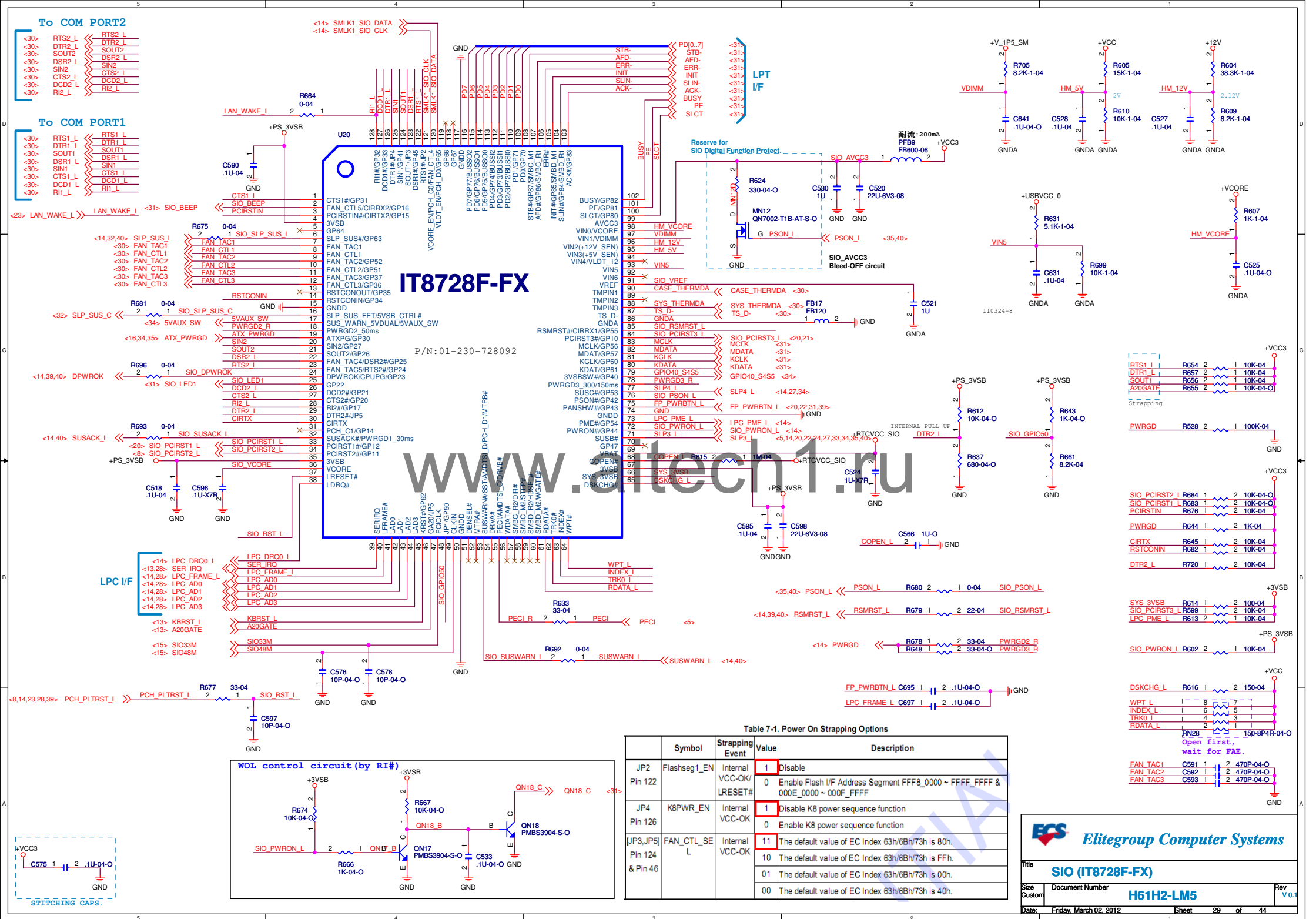
TPM Circuit

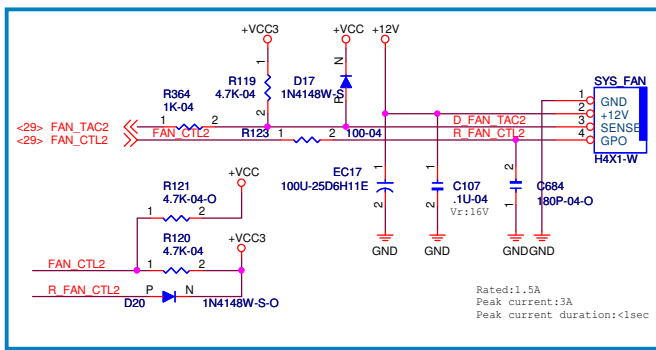
	Ra	Rb	Rc	Rd	Re	Rf	Rg
ST	X	V	V	X	X	X	X
Nuvoton	V	X	X	X	X	V	V

02-440-028262 (default)
ST ST33ZP24AR28PVSC
02-440-421900
NUVOTON NPCT421LA0WX

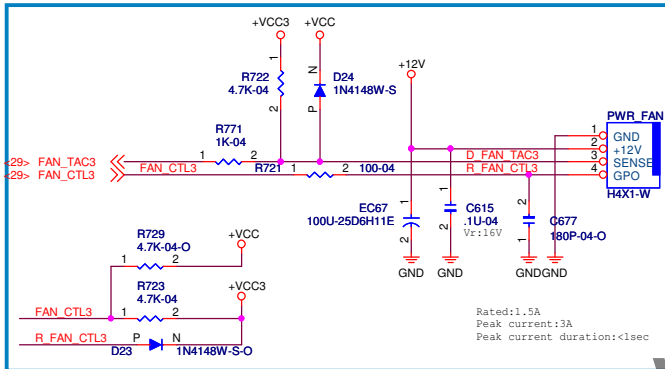


TPM/TCM switching Circuit

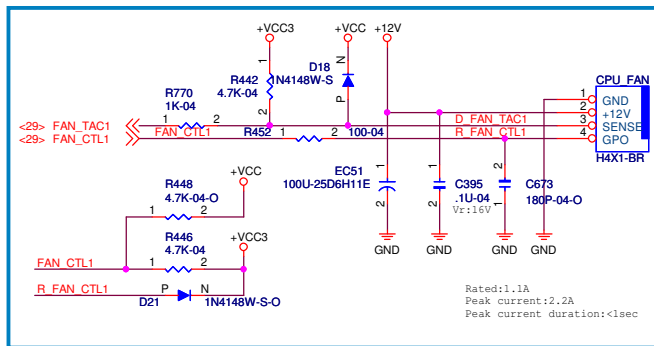




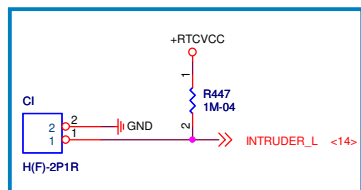
SYS FAN 4-PIN Circuit



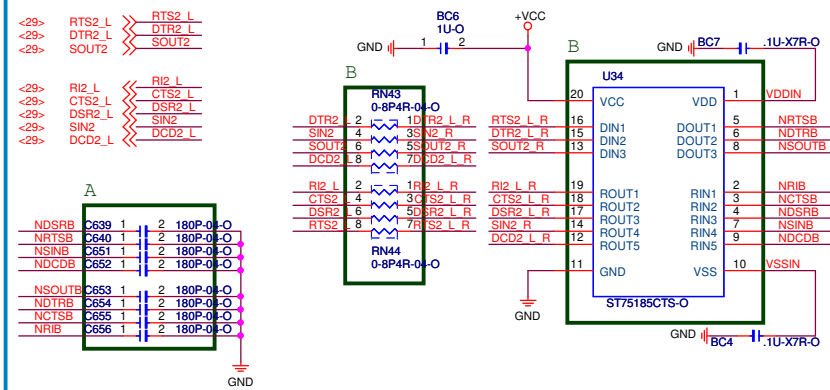
PWR FAN 4-PIN Circuit



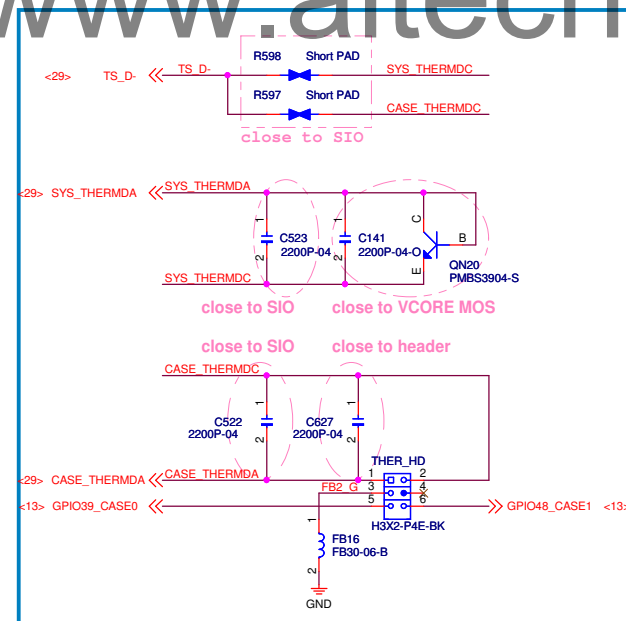
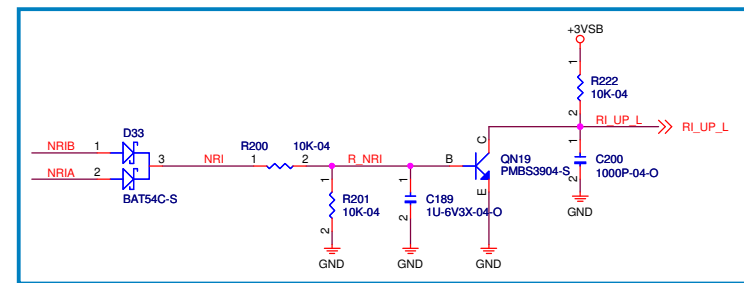
CPU FAN 4-PIN Circuit



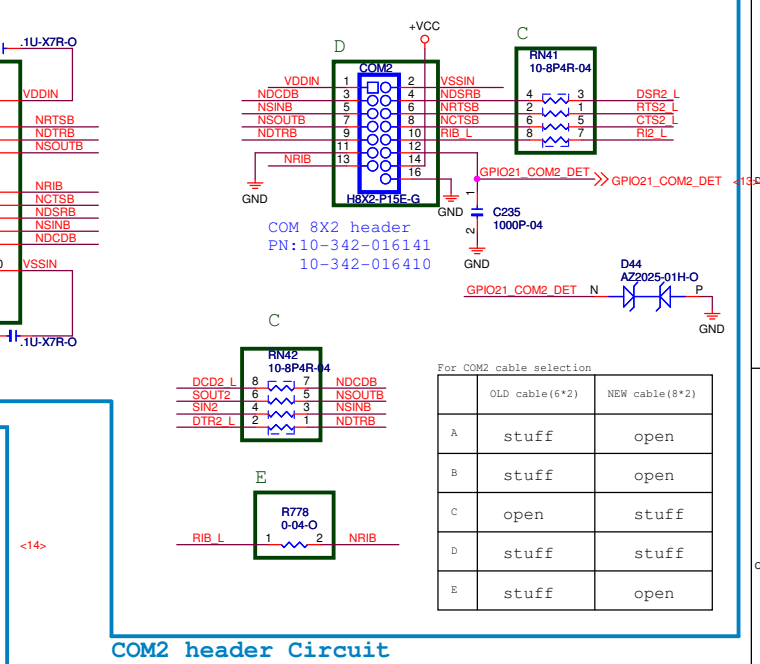
CASE Open Circuit



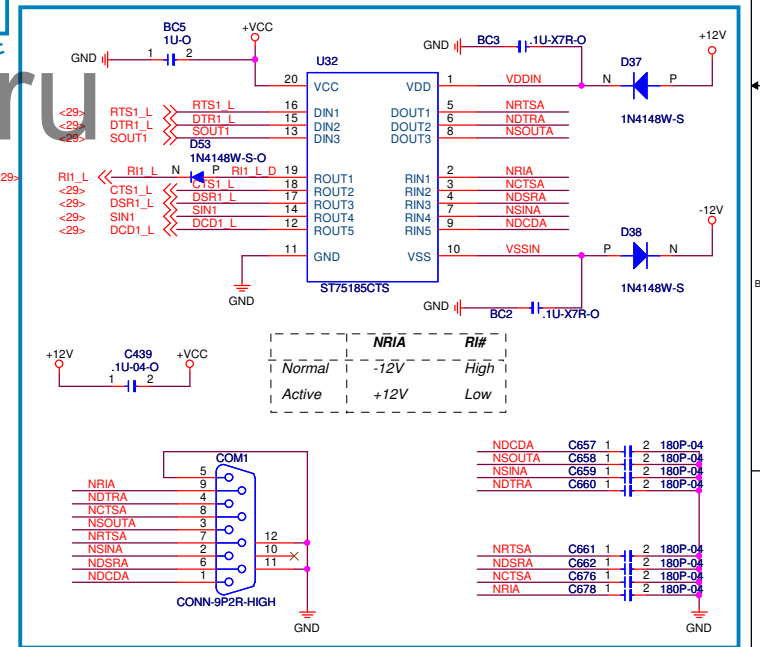
COM RI# Wake Up Circuit



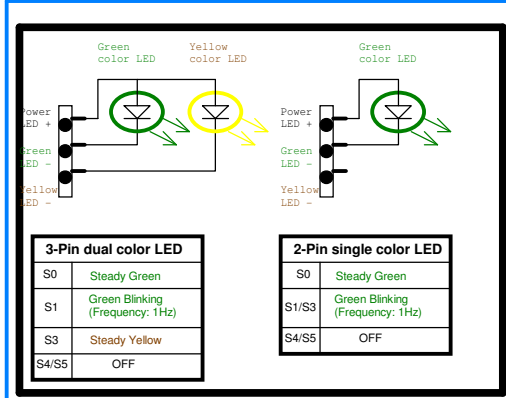
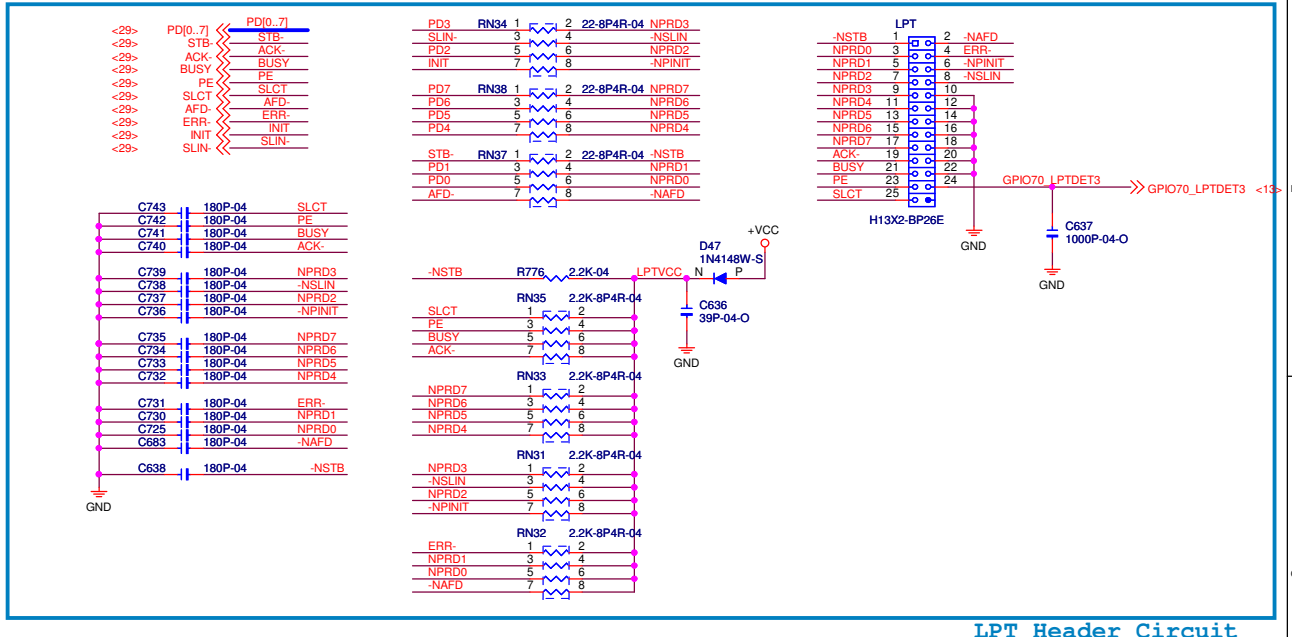
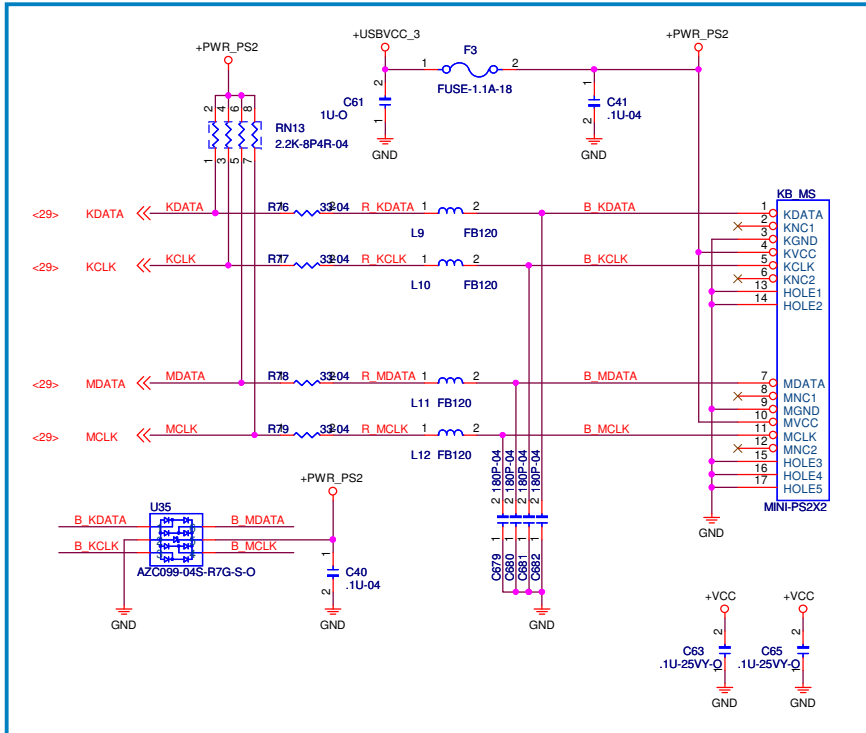
Thermal Sense



COM2 header Circuit

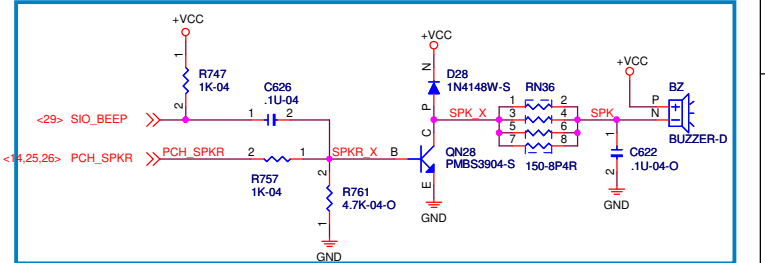
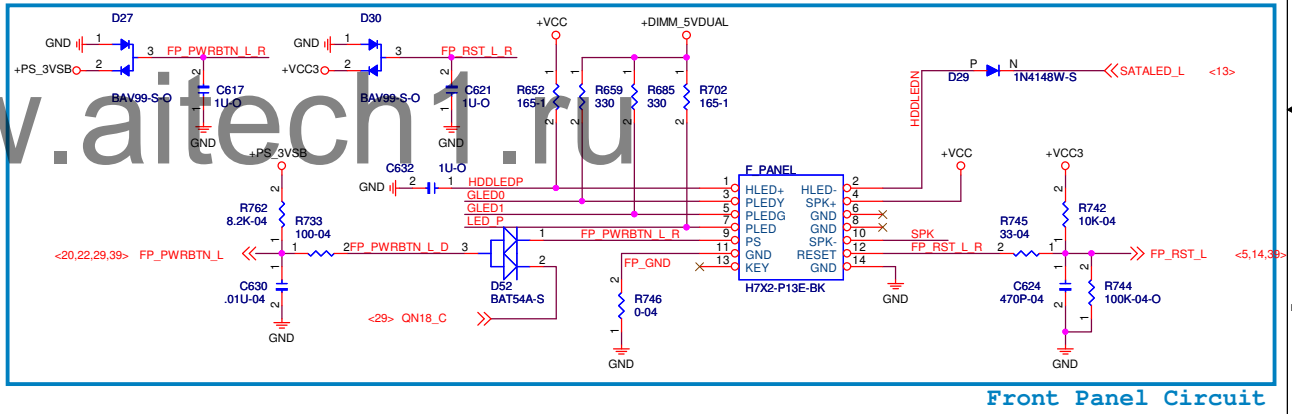
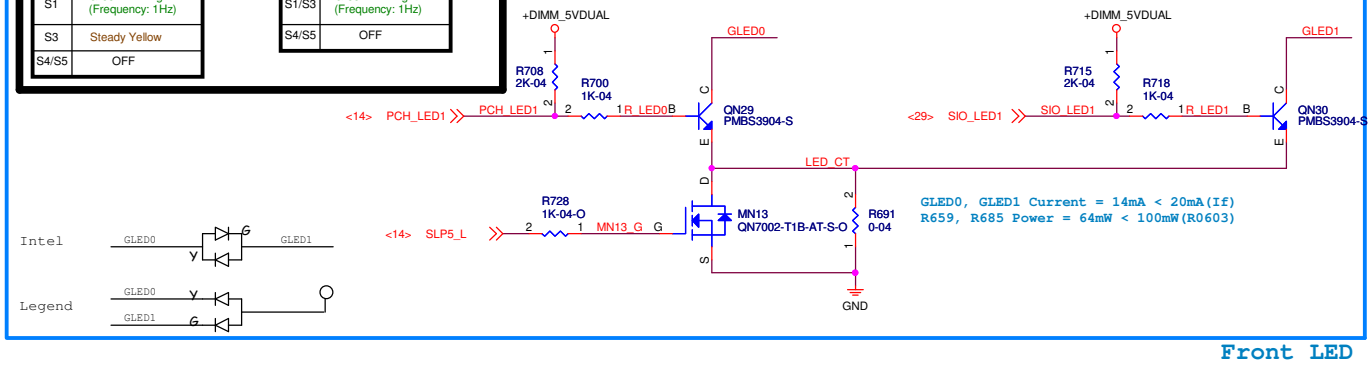


COM1 Rear I/O Circuit



Lenovo LED線路阻値330-06

Source Voltage (V)	5
LED Forward Voltage (V)	1.8
BJT Vce(s) (V)	0
Pull Up Resistor (ohm)	330
LED Forward Current (A)	0.009697
Pull Up Resistor Power (R<1/10 W)	0.03103
LED Power (W)	0.017455

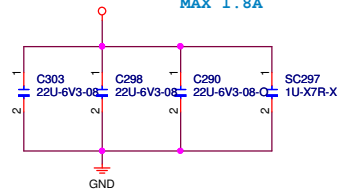




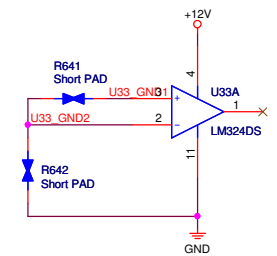
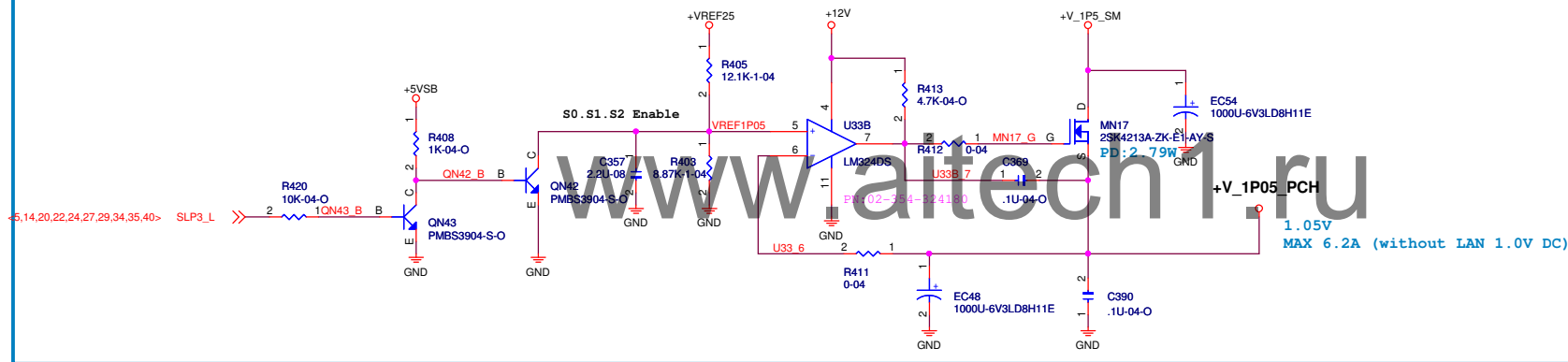
Power Name	Current
4 Slots	0.375 X4 = 1.5A
LAN	16m + 49m = 65mA
LAN	123mA
TPM(WPCT210)	50mA
EPW	16mA
SPI	mA
SIO	mA
Total Current	+ 1.754 A

V1P05 ME

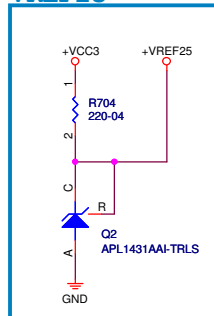
V1.05_ME connect to V1.05_PCH
1.05V
MAX 1.8A



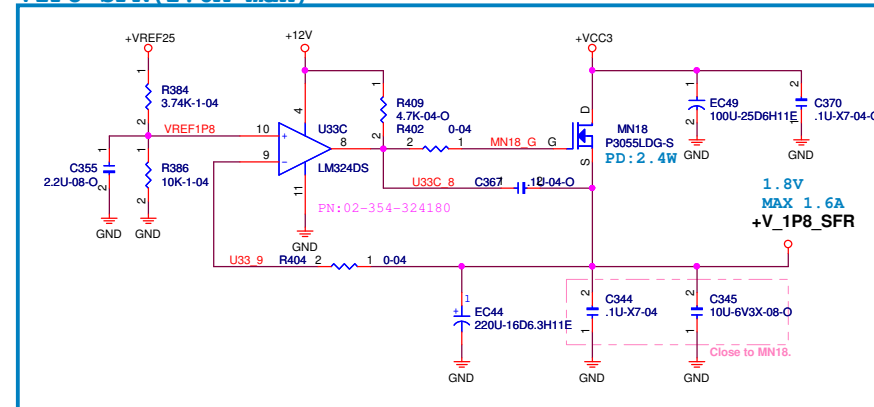
V1P05 PCH



VREF25



V1P8 SFR(1.6A max)

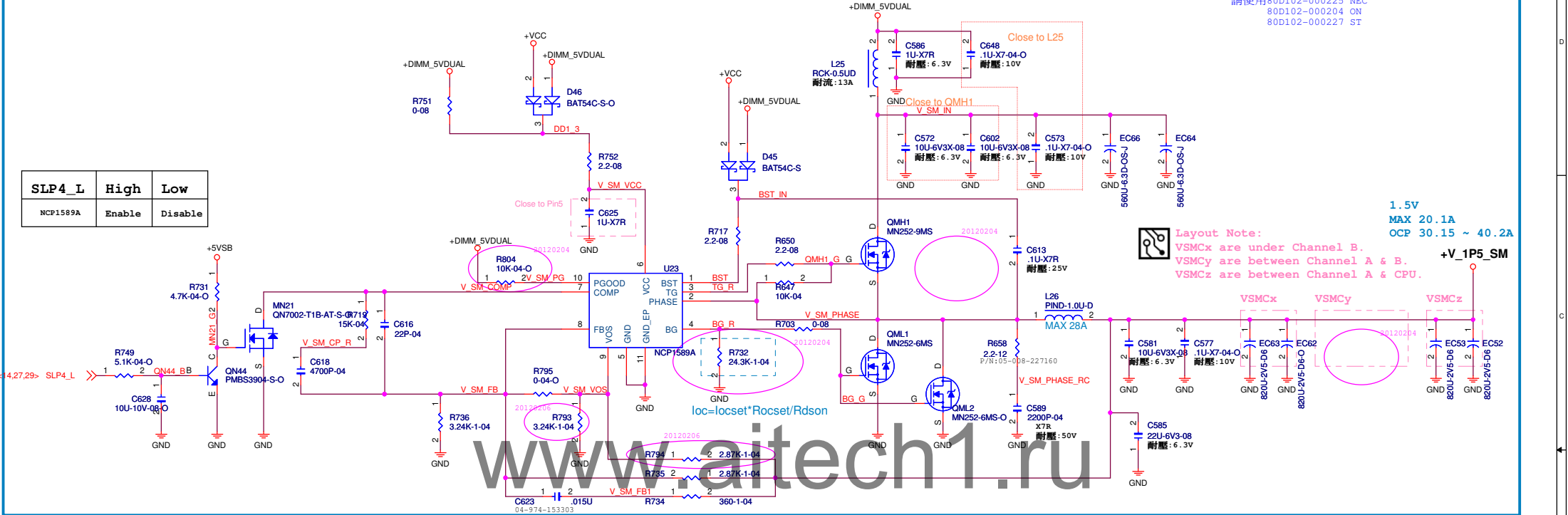


VDIMM

D-PAK selection

Vdimm 1 Phase (上一下一)
請使用 80D102-000225 NEC
80D102-000204 ON
80D102-000227 ST

SLP4_L	High	Low
NCP1589A	Enable	Disable

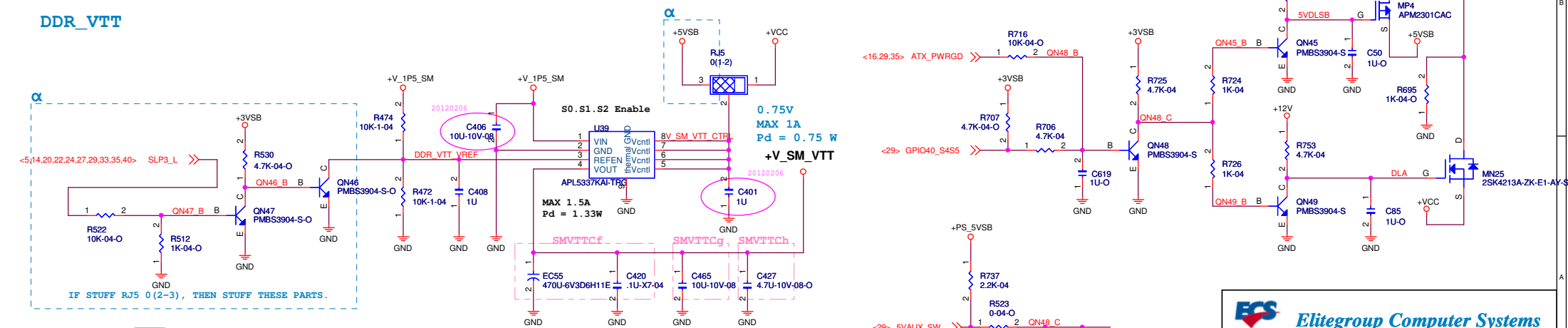


Layout Note:
VSMCx are under Channel B.
VSMCy are between Channel A & B.
VSMCz are between Channel A & CPU.

1.5V
MAX 20.1A
OCP 30.15 ~ 40.2A

DIMM_5VDUAL

DDR_VTT

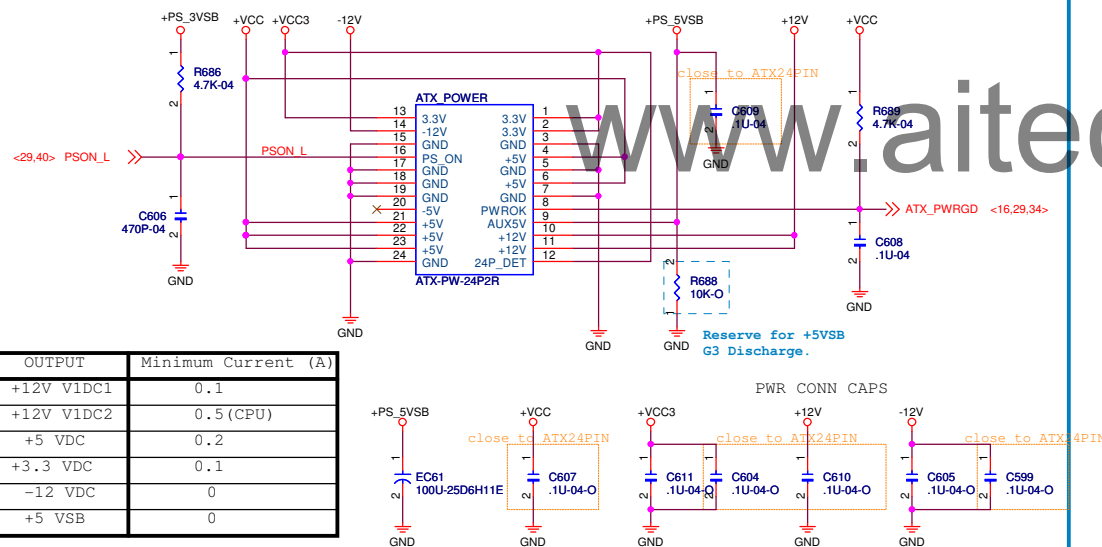
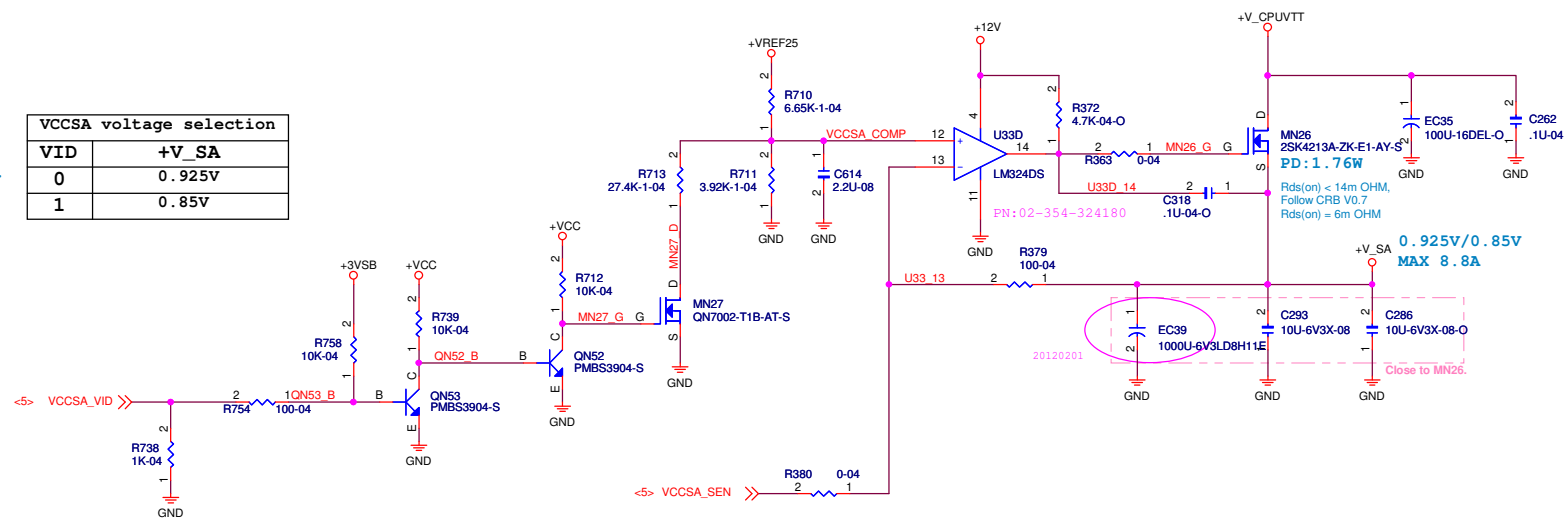


Layout Note:
SMVTTcf close to U39 Pin4.
SMVTTcg are between Channel A & B.
SMVTTCh are between Channel A & CPU.

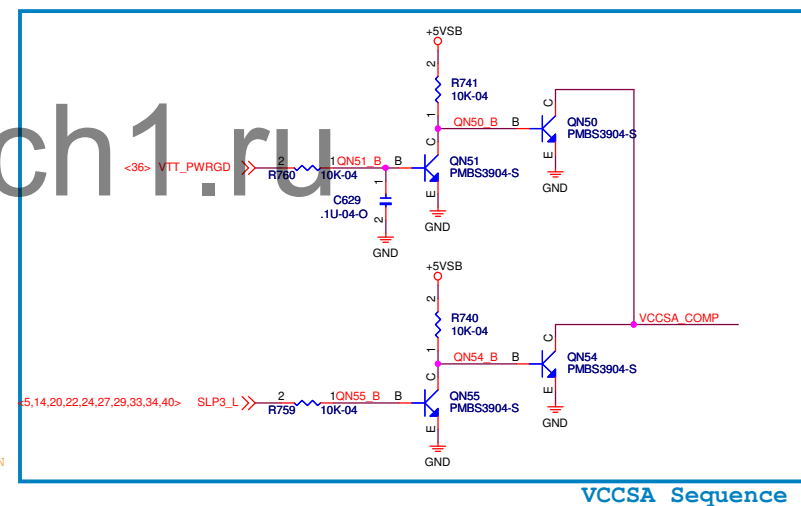
Elitegroup Computer Systems

Title			DC/DC VDIMM/DDR_VTT/5VDUAL
Size	Document Number	H61H2-LM5	
Custom		Rev V0.1	
Date:	Friday, March 02, 2012	Sheet	34 of 44

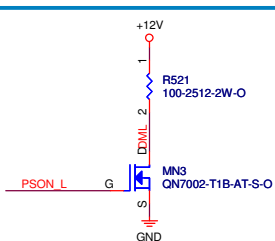
VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V



ATX Power 24PIN

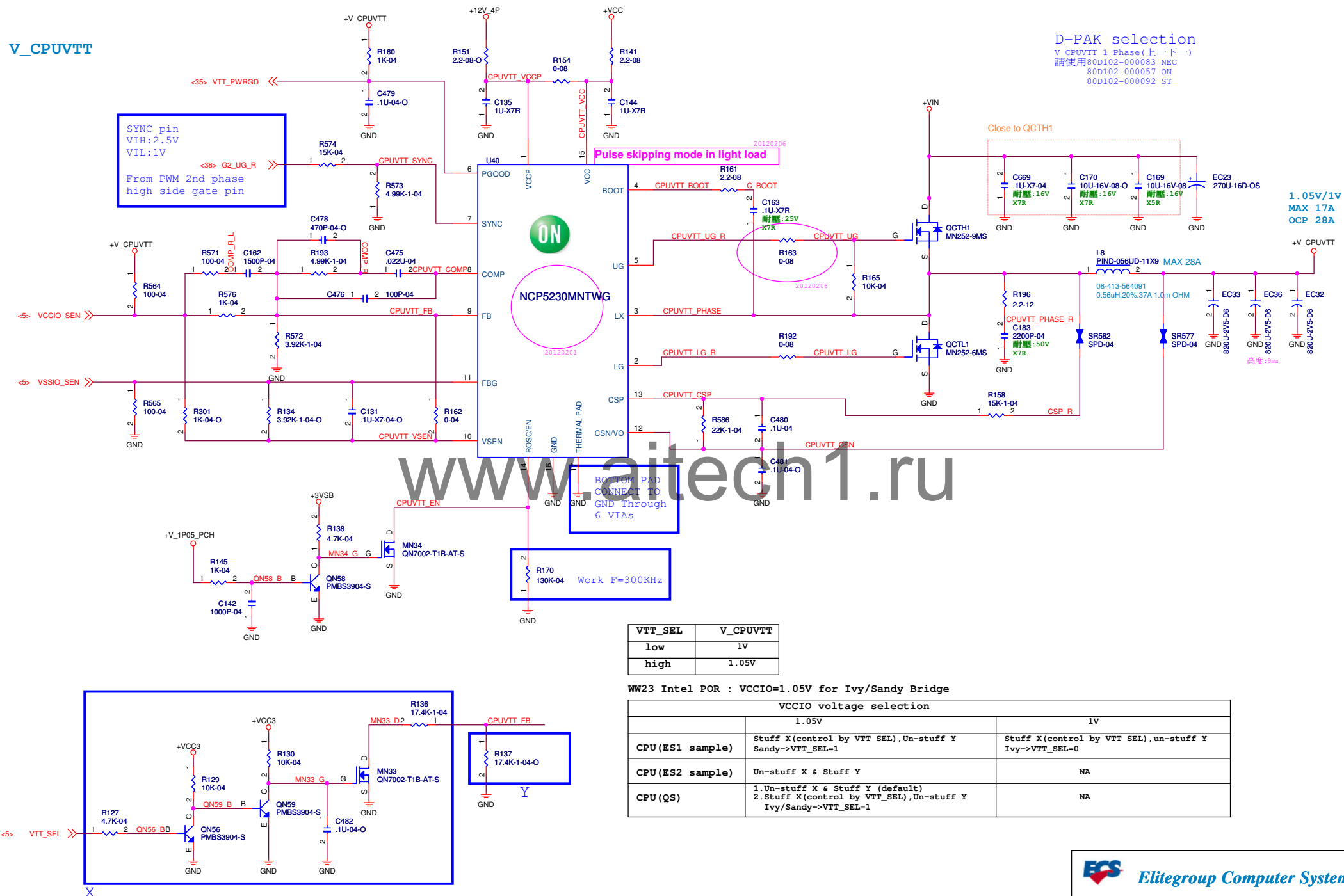


VCCSA Sequence



Dummy Load for Power

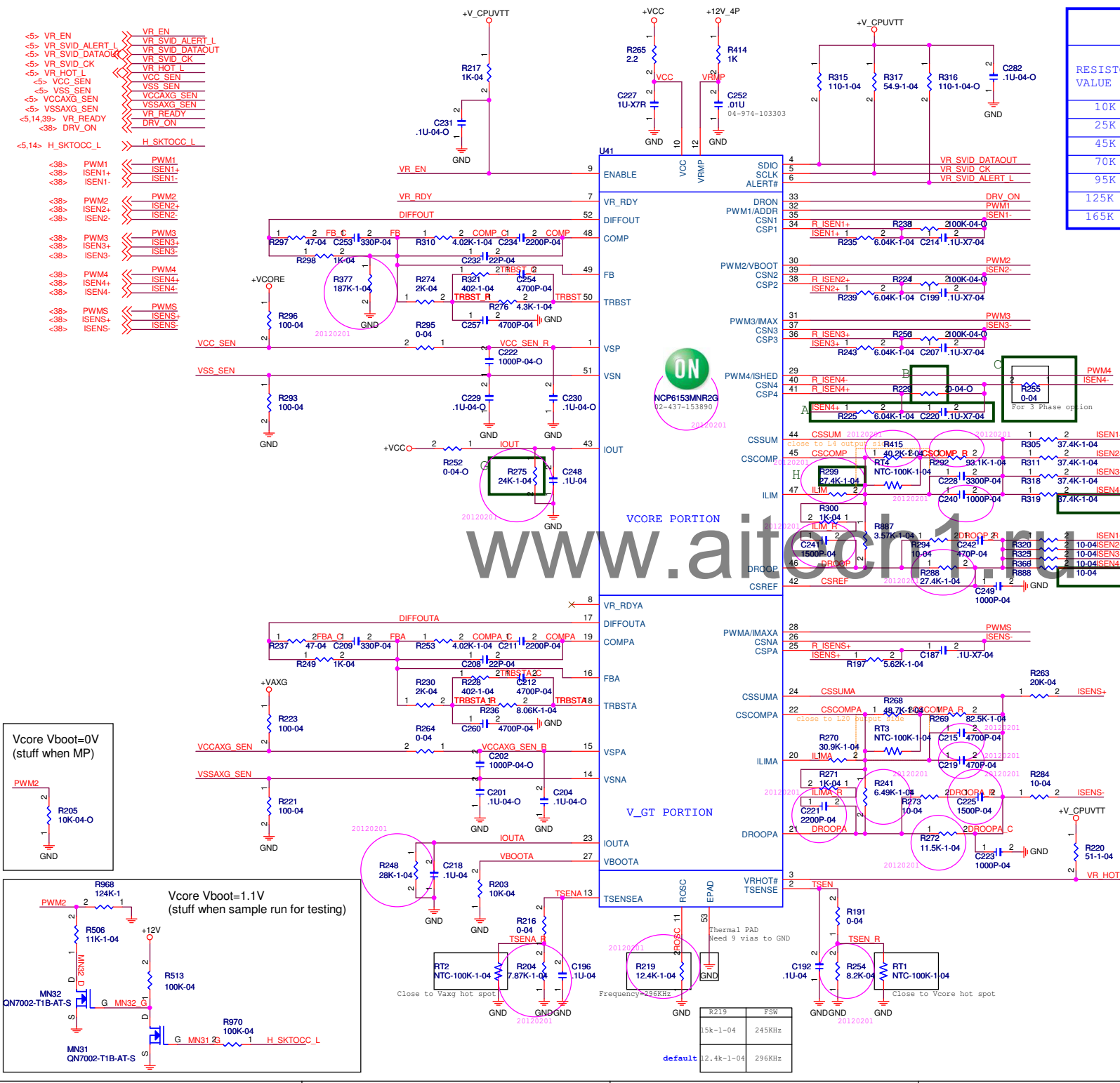
V_CPUVTT



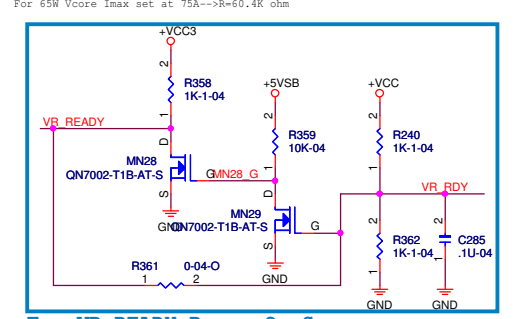
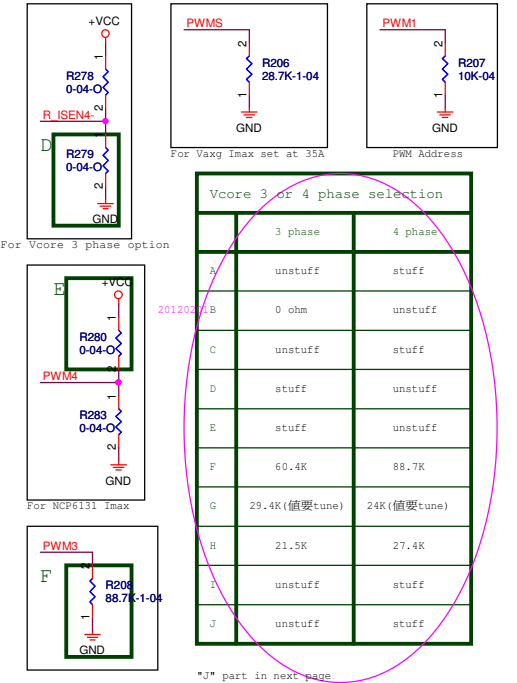
VTT_SEL	V_CPUVTT
low	1V
high	1.05V

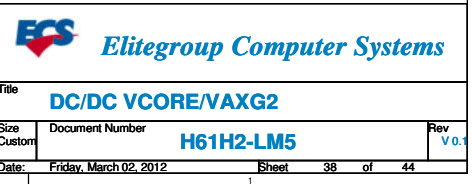
WW23 Intel POR : VCCIO=1.05V for Ivy/Sandy Bridge

VCCIO voltage selection		
	1.05V	1V
CPU(ES1 sample)	Stuff X(control by VTT_SEL),Un-stuff Y Sandy->VTT_SEL=1	Stuff X(control by VTT_SEL),un-stuff Y Ivy->VTT_SEL=0
CPU(ES2 sample)	Un-stuff X & Stuff Y	NA
CPU(QS)	1.Un-stuff X & Stuff Y (default) 2.Stuff X(control by VTT_SEL),Un-stuff Y Ivy/Sandy->VTT_SEL=1	NA



PWM ADDRESS			BOOT VOLTAGE	
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL	RESISTOR VALUE	BOOT VOLTAGE
10K	0000	0001	10K	0V
25K	0010	0011	25K	0.9V
45K	0100	0101	45K	1V
70K	0110	0111	70K	1.1V
95K	1000	1001	95K	1.2V
125K	1010	1011	125K	1.35V
165K	1100	1101	165K	1.5V







PCH Strap Pin

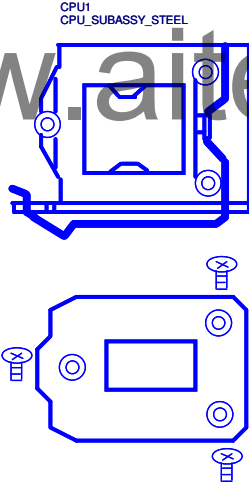
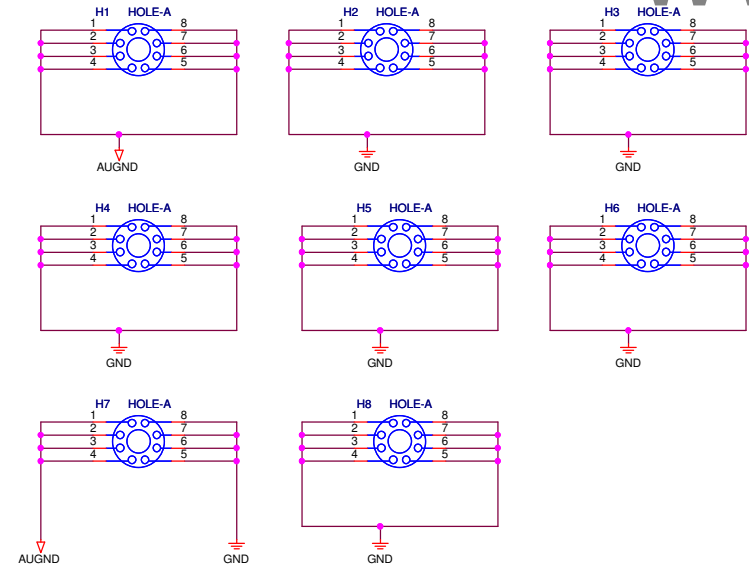
Pin Name	Usage	Default Status
SPKR	No Reboot	20K internal pull-down · No Reboot Mode with TCO Disabled:
INIT3_3V#	Reserved	20K internal pull-up · intend for Firmware Hub.
GNT[3]#/GPIO[55]	Disable Top-Block Swap	20K internal pull-up · “topblock swap” mode Disable
INTVRMEN	Enable Integrated 1.05V VRM	Need External Pull-up · Integrated 1.05V VRM Enable
GNT1# /GPIO51	Boot BIOS Strap bit [1] BBS[1]	20K internal pull-up · The default flash selection is the SPI flash.All
SATA1GP / GPIO19	Boot BIOS Strap bit[0] BBS[0]	20K internal pull-up · The default flash selection is the SPI flash.All
HDA_SDO	Flash Descriptor Security Override/ ME	Internal pull-down. The security measures defined in the Flash Descriptor will be in effect(default)
DF_TV5	Enable DMI termination voltage	This signal has a weak internal pull-down.
GPIO28	Eable On-Die PLL Voltage Regulator	The On-Die PLL voltage regulator is enabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select 1.8V	20K internal pull-down.On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	Enable TLS Confidentiality	Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.

Table 7-1. Power On Strapping Options

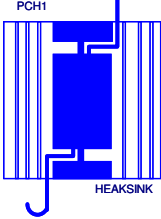
	Symbol	Strapping Event	Value	Description
JP2 Pin 122	Flashseg1_EN	Internal VCC-OK/ LRESET#	1	Disable
			0	Enable Flash I/F Address Segment FFF8_0000 ~ FFFF_FFFF & 000E_0000 ~ 000F_FFFF
JP4 Pin 126	K8PWR_EN	Internal VCC-OK	1	Disable K8 power sequence function
			0	Enable K8 power sequence function
JP3,JP5 Pin 124 & Pin 46	FAN_CTL_SE L	Internal VCC-OK	11	The default value of EC Index 63h/6Bh/73h is 80h.
			10	The default value of EC Index 63h/6Bh/73h is FFh.
			01	The default value of EC Index 63h/6Bh/73h is 00h.
			00	The default value of EC Index 63h/6Bh/73h is 40h.

11-018-115122
SOCKET.CPU...LGA 1155P SMD...15u...BLACK.ACA-ZIF-096-P01...HF.LEAD-FREE.LOTES

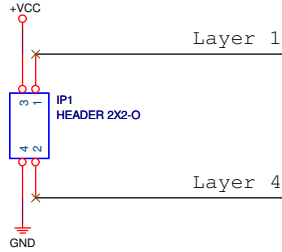
20-800-004611
SUBASSY.STEEL...LGA 1156P...W/BACK PLATE.ACA-ZIF-082-K01...LEAD-FREE (RoHS).LOTES

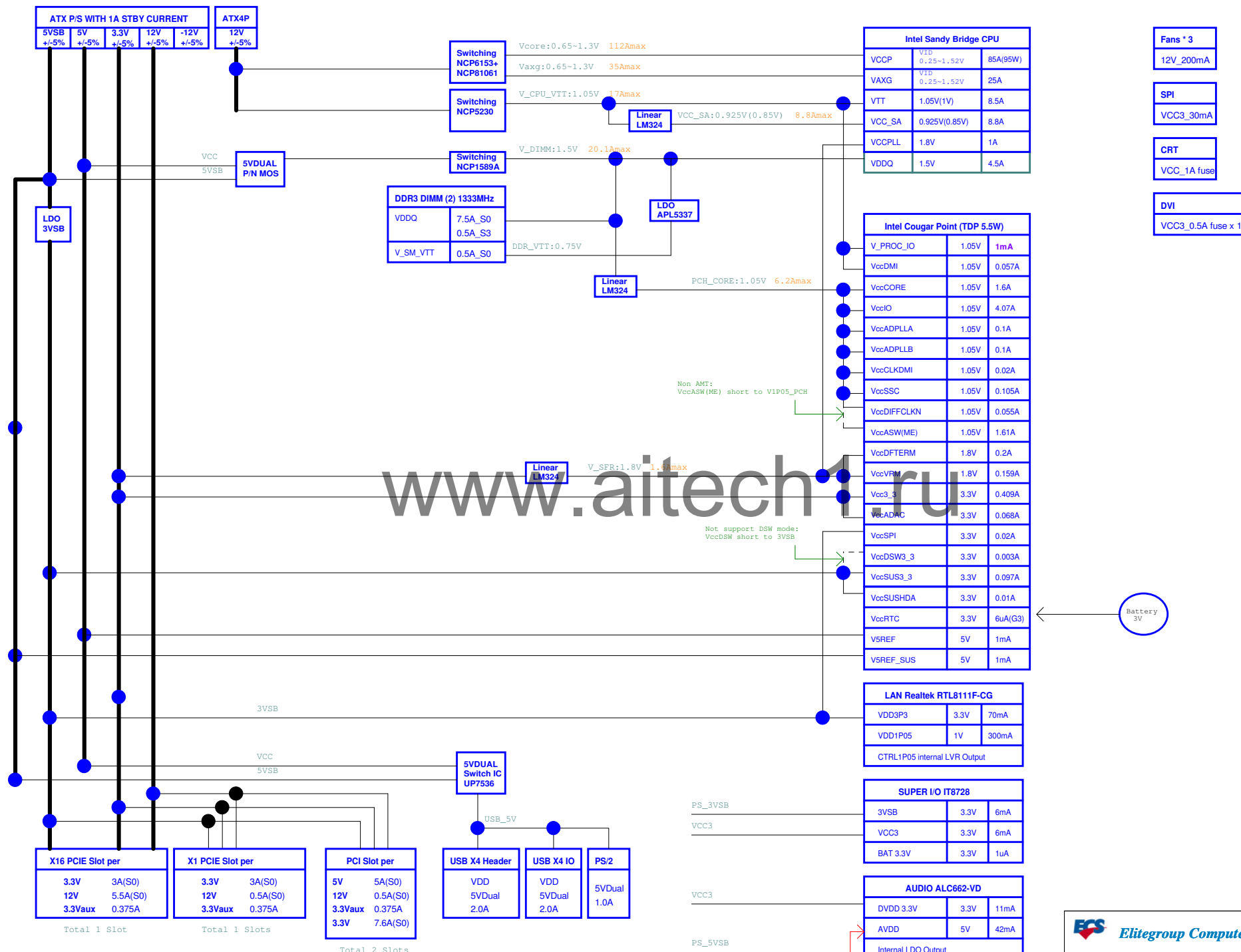


PCH heatsink P/N:
20-120-013526
20-120-013527
20-120-013528 (增加)

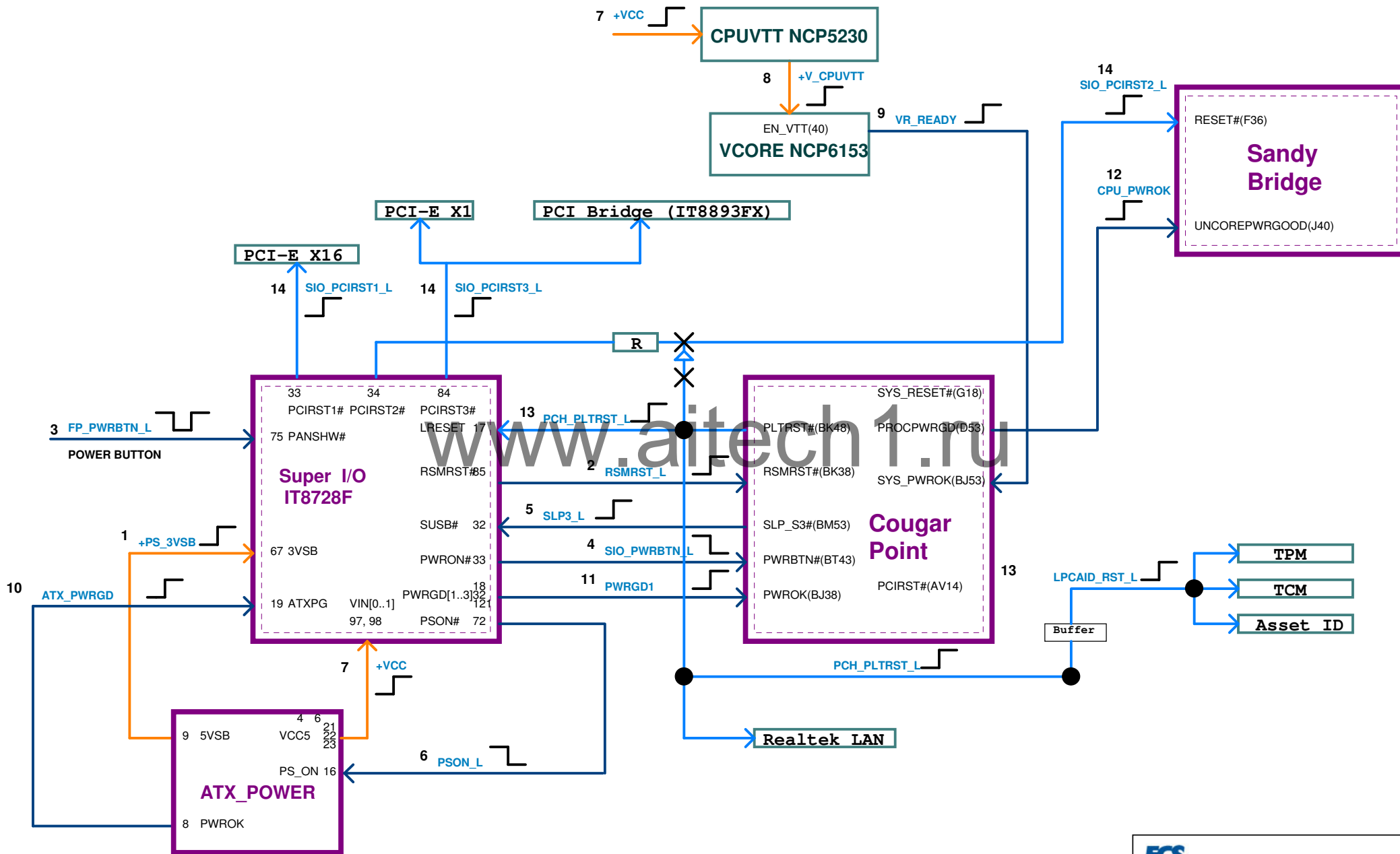


P/N:10-392-002134





www.aitech1.ru



NOTE:

Sugar Bay Platform has two clock mode:

- 1.Integrated Clock Mode (Generate by PCH)
 - 2.Buffer Through Mode (Generate by Clock Gen.)
- If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

